# AHC/AHCT Logic
# Advanced High-Speed CMOS
# Data Book

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## INTRODUCTION

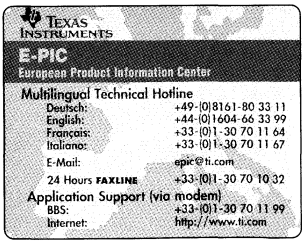
The Advanced High-Speed CMOS (AHC) logic family from Texas Instruments (TI™) provides an effortless migration path for HCMOS users who require higher speed and lower power without paying a noise or price premium. The AHC logic family also offers the broadest selection of logic choices ranging from simple gates/MSI/octals (SN74AHCxxx) to the single-gate (SN74AHC1Gxx) and soon-to-be-released Widebus™ (SN74AHC16xxx) devices. Add to that the ability to operate at both 3.3 V and 5 V and you have a reliable migration path from HCMOS.

Performance characteristics of the AHC family are:

- **Low noise** – The AHC family allows designers to maintain the same low noise characteristics of HCMOS without the overshoot and undershoot typical of higher-drive devices usually required to achieve AHC speeds.
- **Low power** – The AHC family, by using CMOS technology, has low power consumption (40-μA maximum static current, one-half that of HCMOS).
- **Speed** – With typical propagation delays of 5.2 ns (octals), AHC offers three times the speeds of HCMOS.
- **Drive** – Output-drive current is ±8 mA at 5-V $V_{CC}$ and ±4-mA at 3.3-V $V_{CC}$.
- **5-V input tolerance at 3.3 V** – With the input diode to $V_{CC}$ removed, AHC is specified for both 5-V and 3.3-V operation.
- **Pin-for-pin compatibility** – All AHC devices are pin-for-pin compatible with industry-standard functional pinouts.
- **Options** – With CMOS- (AHC) and TTL- (AHCT) compatible devices available in gates/MSI/octals, single gates, and soon-to-be-released Widebus, the AHC family offers the widest selection of logic choices on the market.
- **Packaging** – AHC devices are available in D and DW (SOIC), N (PDIP), DB (SSOP), PW (TSSOP), DGV (TVSOP), and DBV (SOT) packages, and are planned in a variety of Widebus package offerings. Selected AHC devices are available in military versions (SN54AHCxx).

For more information on these or other TI products, please contact your local TI representative, authorized distributor, the European Product Information Centre, or visit the TI logic home page at http://www.ti.com/sc/logic.

For a complete listing of all TI logic products, please order our logic CD-ROM (literature number SCBC001) or Logic Selection Guide (literature number SDYU001) by contacting our European Product Information Centre.



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## Contents

## INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

### operating conditions and characteristics (in sequence by letter symbols)

**$C_i$** **Input capacitance**

The internal capacitance at an input of the device

**$C_{io}$** **Input/output capacitance**

Input-to-output internal capacitance; transcapacitance

**$C_o$** **Output capacitance**

The internal capacitance at an output of the device

**$C_{pd}$** **Power dissipation capacitance**

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$

**$f_{max}$** **Maximum clock frequency**

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification

**$I_{CC}$** **Supply current**

The current into* the $V_{CC}$ supply terminal of an integrated circuit

**$\Delta I_{CC}$** **Supply current change**

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$

**$I_{CEX}$** **Output high leakage current**

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition $V_O = 5.5$ V

**$I_{I(hold)}$** **Input hold current**

Input current that holds the input at the previous state when the driving device goes to a high-impedance state

**$I_{IH}$** **High-level input current**

The current into* an input when a high-level voltage is applied to that input

**$I_{IL}$** **Low-level input current**

The current into* an input when a low-level voltage is applied to that input

**$I_{off}$** **Input/output power-off leakage current**

The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and $V_{CC} = 0$ V

**$I_{OH}$** **High-level output current**

The current into* an output with input conditions applied that, according to the product specification, establishes a high level at the output

*Current out of a terminal is given as a negative value.

$I_{OL}$ **Low-level output current**

The current into* an output with input conditions applied that, according to the product specification, establishes a low level at the output

$I_{OZ}$, $I_{OZPU/PD}$ **Off-state (high-impedance-state) output current (of a 3-state output)**

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, establishes the high-impedance state at the output

$t_a$ **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output

$t_c$ **Clock cycle time**

Clock cycle time is $1/f_{max}$.

$t_{dis}$ **Disable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or $t_{PLZ}$. Open-collector outputs change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.

$t_{en}$ **Enable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low)

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or $t_{PZL}$. Open-collector outputs change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

$t_h$ **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

$t_{pd}$ **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or $t_{PLH}$)

$t_{PHL}$ **Propagation delay time, high-to-low level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

$t_{PHZ}$ **Disable time (of a 3-state output) from high level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

*Current out of a terminal is given as a negative value.

$t_{PLH}$ **Propagation delay time, low-to-high level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

$t_{PLZ}$ **Disable time (of a 3-state output) from low level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

$t_{PZH}$ **Enable time (of a 3-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

$t_{PZL}$ **Enable time (of a 3-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

$t_{sk(o)}$ **Output skew**

The difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching output. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.

$t_{su}$ **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is to be expected.

$t_w$ **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

$V_{IH}$ **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

$V_{IL}$ **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

$V_{OH}$ **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output

**$V_{OL}$** **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output

**$V_{IT+}$** **Positive-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, $V_{IT-}$

**$V_{IT-}$** **Negative-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, $V_{IT+}$

The following symbols are used in function tables on TI data sheets:

| | | |
|---|---|---|
| H | = | high level (steady state) |
| L | = | low level (steady state) |
| ↑ | = | transition from low to high level |
| ↓ | = | transition from high to low level |
| → | = | value/level or resulting value/level is routed to indicated destination |
| ↶ | = | value/level is re-entered |
| X | = | irrelevant (any input, including transitions) |
| Z | = | off (high-impedance) state of a 3-state output |
| a . . . h | = | the level of steady-state inputs A through H, respectively |
| $Q_0$ | = | level of Q before the indicated steady-state input conditions were established |
| $\overline{Q}_0$ | = | complement of $Q_0$ or level of $\overline{Q}$ before the indicated steady-state input conditions were established |
| $Q_n$ | = | level of Q before the most recent active transition indicated by ↓ or ↑ |
| ⎍ | = | one high-level pulse |
| ⎾ | = | one low-level pulse |
| Toggle | = | each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑ |

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, $Q_0$, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎾, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

## EXPLANATION OF FUNCTION TABLES

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register.

**FUNCTION TABLE**

| INPUTS | | | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLEAR | MODE | | CLOCK | SERIAL | | PARALLEL | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| | S1 | S0 | | LEFT | RIGHT | A | B | C | D | | | | |
| L | X | X | X | X | X | X | X | X | X | L | L | L | L |
| H | X | X | L | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| H | H | H | ↑ | X | X | a | b | c | d | a | b | c | d |
| H | L | H | ↑ | X | H | H | H | H | H | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | L | H | ↑ | X | L | L | L | L | L | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | H | L | ↑ | H | X | X | X | X | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | H |
| H | H | L | ↑ | L | X | X | X | X | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | L |
| H | L | L | X | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs occurs while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A is at output $Q_A$, data entered at B is at $Q_B$, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at $Q_A$ is now at $Q_B$, the previous levels of $Q_B$ and $Q_C$ are now at $Q_C$ and $Q_D$, respectively, and the data previously at $Q_D$ is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at $Q_B$ is now at $Q_A$, the previous levels of $Q_C$ and $Q_D$ are now at $Q_B$ and $Q_C$, respectively, and the data previously at $Q_A$ is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

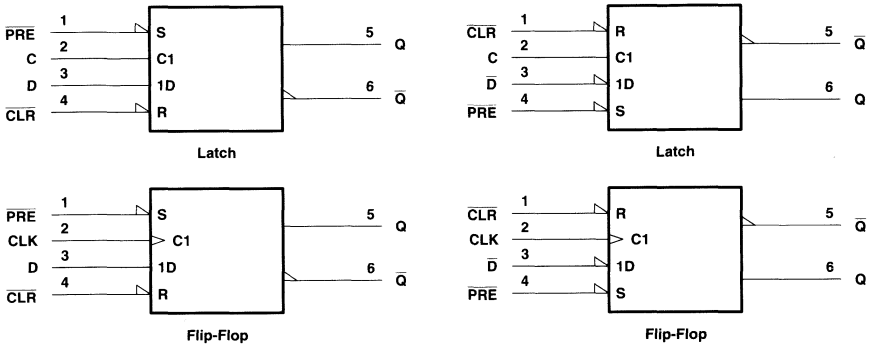
The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

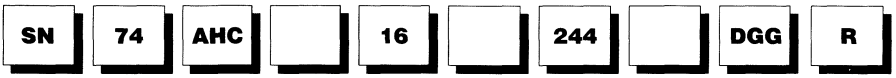
In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.




The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators ( ▷ ) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

# DEVICE NAMES AND PACKAGE DESIGNATORS

***Example:***




### *1 Standard Prefix*

Example: SNJ – Conforms to MIL-PRF-38535 (QML)

### *2 Temperature Range*

Examples: 54 – Military
74 – Commercial

### *3 Family*

Examples: Blank – Transistor-Transistor Logic
ABT – Advanced BiCMOS Technology
ABTE – Advanced BiCMOS Technology/ Enhanced Transceiver Logic
AC/ACT – Advanced CMOS Logic
AHC/AHCT – Advanced High-Speed CMOS Logic
ALS – Advanced Low-Power Schottky Logic
AS – Advanced Schottky Logic
ALVC – Advanced Low-Voltage CMOS Technology
BCT – BiCMOS Bus-Interface Technology
CBT – Crossbar Technology
F – F Logic
FB – Backplane Transceiver Logic/Futurebus+
GTL – Gunning Transceiver Logic
HC/HCT – High-Speed CMOS Logic
LS – Low-Power Schottky Logic
LV – Low-Voltage HCMOS Technology
LVC – Low-Voltage CMOS Technology
LVT – Low-Voltage BiCMOS Technology
S – Schottky Logic
SSTL – Stub Series Terminated Logic

### *4 Special Features*

Examples: Blank = No Special Features
D – Level-Shifting Diode (CBTD)
H – Bus Hold (ALVCH)
R – Damping Resistor on Inputs/Outputs (LVCR)
S – Schottky Clamping Diode (CBTS)

### *5 Bit Width*

Examples: Blank = Gates, MSI, and Octals
1G – Single Gate
8 – Octal IEEE 1149.1 (JTAG)
16 – Widebus™ (16, 18, and 20 bit)
18 – Widebus IEEE 1149.1 (JTAG)
32 – Widebus+™ (32 and 36 bit)

### *6 Options*

Examples: Blank = No Options
2 – Series-Damping Resistor on Outputs
4 – Level Shifter
25 – 25-Ω Line Driver

### *7 Function*

Examples: 244 – Noninverting Octal Buffer/Driver
374 – Octal D-Type Flip-Flop
573 – D-Type Transparent Latch
640 – Inverting Octal Transceiver

### *8 Device Revision*

Examples: Blank = No Revision
Letter Designator A–Z

### *9 Packages*

Examples: D, DW – Small-Outline Integrated Circuit (SOIC)
DB, DL – Shrink Small-Outline Package (SSOP)
DBB, DGV – Thin Very Small-Outline Package (TVSOP)
DBV – Small-Outline Transistor Package (SOT)
DGG, PW – Thin Shrink Small-Outline Package (TSSOP)
FK – Leadless Ceramic Chip Carrier (LCCC)
FN – Plastic Leaded Chip Carrier (PLCC)
GB – Ceramic Pin Grid Array (CPGA)
HFP, HS, HT, HV – Ceramic Quad Flat Package (CQFP)
J, JT – Ceramic Dual-In-Line Package (CDIP)
N, NP, NT – Plastic Dual-In-Line Package (PDIP)
PAG, PAH, PCA, PCB, PM, PN, PZ – Plastic Thin Quad Flat Package (TQFP)
PH, PQ, RC – Plastic Quad Flat Package (QFP)
W, WA, WD – Ceramic Flat Package (CFP)

### *10 Tape and Reel*

Examples: LE – Left Embossed (required for DB and PW packages)
R – Standard (required for DGG, DBB, DGV, and DBV; optional for D, DL, and DW packages)

In digital-system design, consideration must be given to thermal management of components. The small size of the small-outline packages makes this even more critical. Figures 1–5 show the thermal resistance for the small-outline 14-, 16-, 20-, 24-, and 48-pin packages for various rates of airflow calculated in accordance with JESD 51.

The thermal resistances in Figures 1–5 can be used to approximate typical and maximum virtual junction temperatures. In general, the junction temperature for any device can be calculated using the following equation:

$$T_J = R_{\theta JA} \times P_T + T_A$$

where:

$T_J$ = virtual junction temperature (°C)
$R_{\theta JA}$ = thermal resistance, junction to free air (°C/W)
$P_T$ = total power dissipation of the device (W)
$T_A$ = free-air temperature (°C)

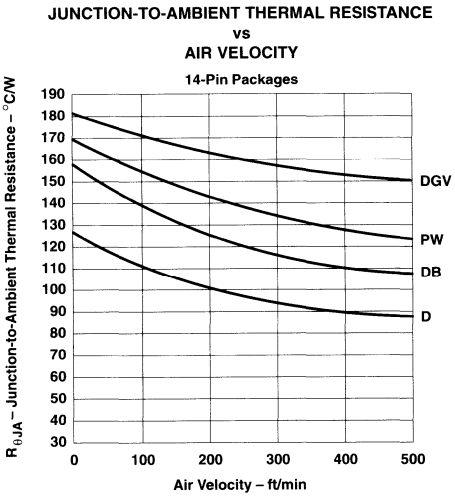



**Figure 1**

JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
AIR VELOCITY
16-Pin Packages

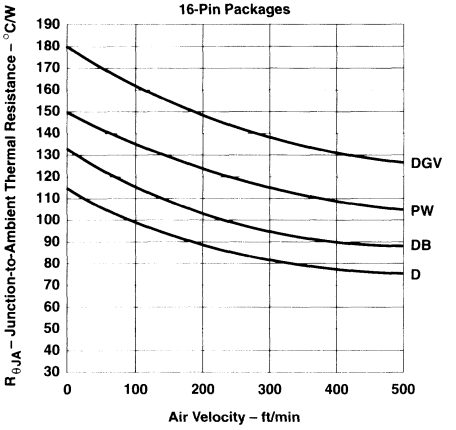



Figure 2

JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
AIR VELOCITY
20-Pin Packages

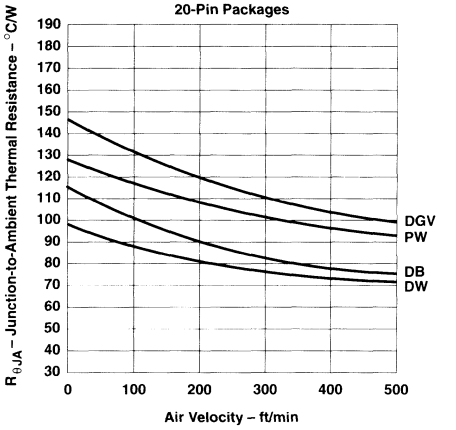



Figure 3

JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
AIR VELOCITY
24-Pin Packages

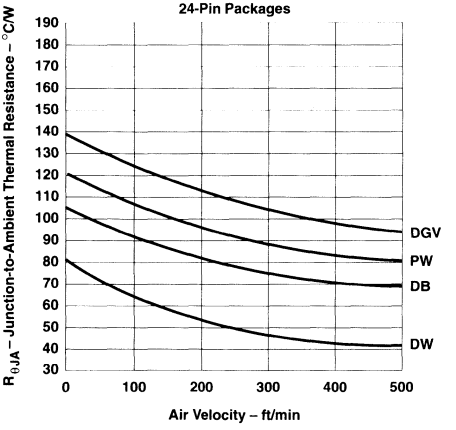



Figure 4

JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
AIR VELOCITY
48-Pin Packages

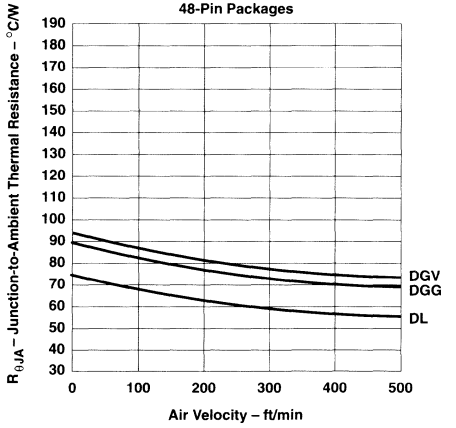
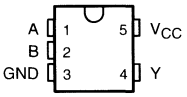



Figure 5

## Contents

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




## description

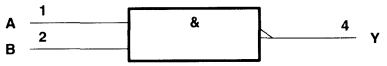
The SN74AHC1G00 performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74AHC1G00 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

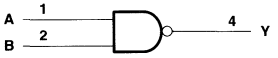
| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




EPIC is a trademark of Texas Instruments Incorporated.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.44 | |
| $I_I$ | A or B inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | 10 | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5.5 | 7.9 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8 | 11.4 | 1 | 13 | |

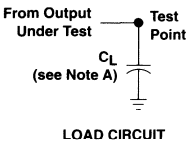
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 3.7 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.7 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.2 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.2 | 7.5 | 1 | 8.5 | |

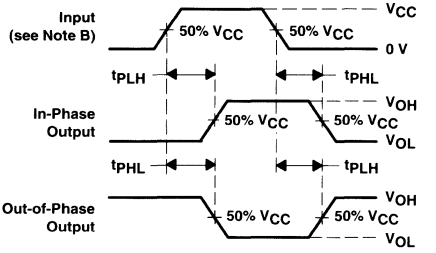
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 9.5 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

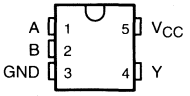
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

SCLS316D – MARCH 1996 – REVISED JUNE 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




## description

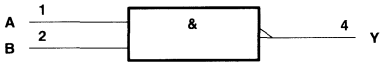
The SN74AHCT1G00 performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74AHCT1G00 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

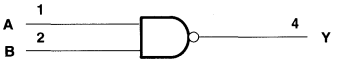
| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




EPIC is a trademark of Texas Instruments Incorporated.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

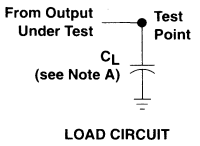
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 6.9 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9 | |

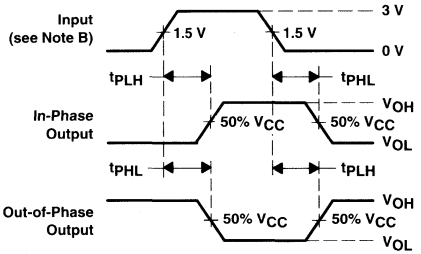
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 10.5 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

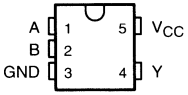
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

SCLS342C – APRIL 1996 – REVISED JUNE 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




## description

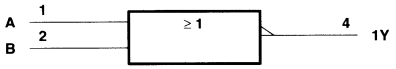
This device contains a single 2-input NOR gate that performs the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

The SN74AHC1G02 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

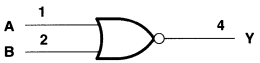
| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| H | X | L |
| X | H | L |
| L | L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




EPIC is a trademark of Texas Instruments Incorporated.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I < 0$) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | 10 | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5.6 | 7.9 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 7.9 | 1 | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.1 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.4 | 1 | 13 | |

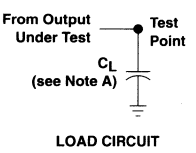
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 3.6 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.6 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.1 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.1 | 7.5 | 1 | 8.5 | |

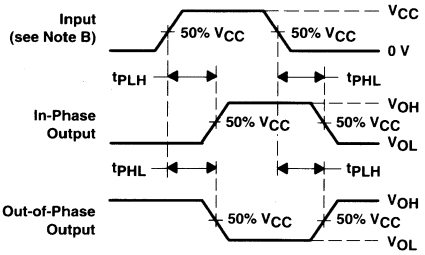
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per gate | No load, | f = 1 MHz | 15 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



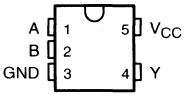

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




## description

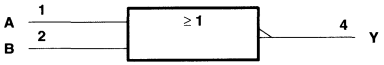
This device contains a single 2-input NOR gate that performs the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

The SN74AHCT1G02 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

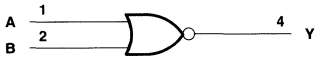
| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | X | L |
| X | H | L |
| L | L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




EPIC is a trademark of Texas Instruments Incorporated.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | | 4.5 V | 4.4 | 4.5 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | | 4.5 V | | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | | 5.5 V | | | ±0.1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | | 1 | | 10 | µA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, | Other inputs at GND or $V_{CC}$ | 5.5 V | | | 1.35 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | | 5 V | | 4 | 10 | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

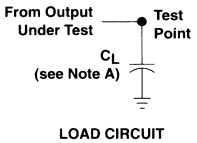
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 2.4 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.5 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 3.4 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 4.5 | 7.5 | 1 | 8.5 | |

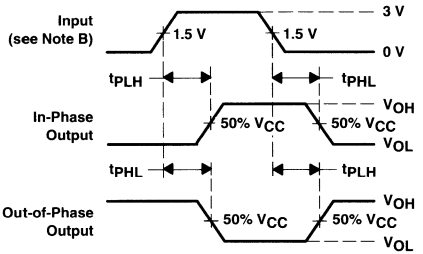
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 17 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

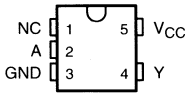
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

SCLS318D – MARCH 1996 – REVISED JUNE 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

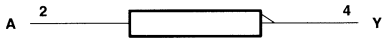
The SN74AHC1G04 contains one inverter gate. The device performs the Boolean function $Y = \overline{A}$.

The SN74AHC1G04 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

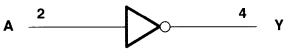
| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




EPIC is a trademark of Texas Instruments Incorporated.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | 10 | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5 | 7.1 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5 | 7.1 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.5 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.5 | 10.6 | 1 | 12 | |

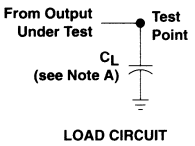
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |

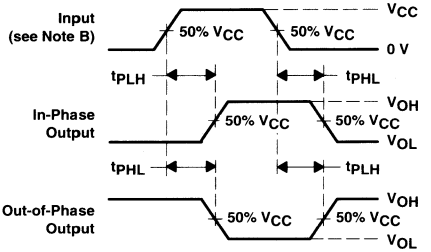
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 12 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

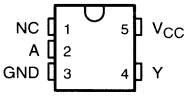
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

SCLS343F – APRIL 1996 – REVISED JUNE 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Unbuffered Output**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

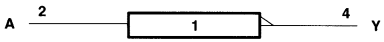
The SN74AHC1GU04 contains a single inverter gate. The device performs the Boolean function $Y = \overline{A}$. Internal circuitry consists of a single-stage inverter that can be used in analog applications, such as crystal oscillators.

The SN74AHC1GU04 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

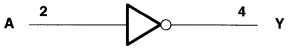
| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




EPIC is a trademark of Texas Instruments Incorporated.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.7 | | V |
| | | $V_{CC}$ = 3 V | 2.4 | | |
| | | $V_{CC}$ = 5.5 V | 4.4 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.3 | V |
| | | $V_{CC}$ = 3 V | | 0.6 | |
| | | $V_{CC}$ = 5.5 V | | 1.1 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.8 | 2 | | 1.8 | | V |
| | | 3 V | 2.7 | 3 | | 2.7 | | |
| | | 4.5 V | 4 | 4.5 | | 4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.2 | | 0.2 | V |
| | | 3 V | | | 0.3 | | 0.3 | |
| | | 4.5 V | | | 0.5 | | 0.5 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | 10 | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | OUTPUT CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5 | 8.9 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5 | 8.9 | 1 | 10.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.5 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 7.5 | 11.4 | 1 | 13 | |

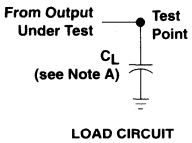
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | OUTPUT CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.5 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.5 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5 | 7 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 7 | 1 | 8 | |

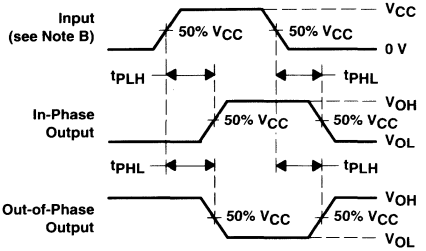
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 7.3 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

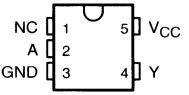
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

SCLS319E – MARCH 1996 – REVISED JUNE 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

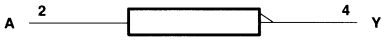
The SN74AHCT1G04 contains one gate. The device performs the Boolean function $Y = \overline{A}$.

The SN74AHCT1G04 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

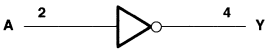
| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




EPIC is a trademark of Texas Instruments Incorporated.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | | 4.5 V | 4.4 | 4.5 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | | 4.5 V | | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | | 5.5 V | | | ±0.1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | | 1 | | 10 | µA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | | 5 V | | 4 | 10 | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

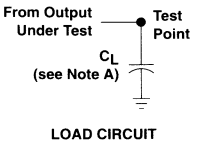
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 4.7 | 6.7 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 4.7 | 6.7 | 1 | 7.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.5 | 7.7 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.7 | 1 | 8.5 | |

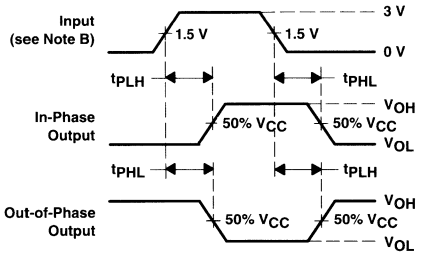
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 14 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

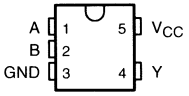
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

SCLS314C – MARCH 1996 – REVISED JUNE 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




## description

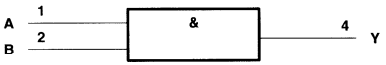
The SN74AHC1G08 is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN74AHC1G08 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

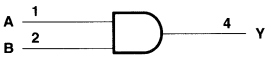
| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




EPIC is a trademark of Texas Instruments Incorporated.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.44 | |
| $I_I$ | A or B inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | 10 | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | OUTPUT CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 6.2 | 8.8 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.2 | 8.8 | 1 | 10.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 8.7 | 12.3 | 1 | 14 | |

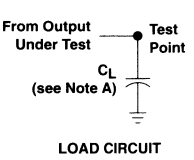
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | OUTPUT CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 4.3 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$ | | | | | 4.3 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.8 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.8 | 7.9 | 1 | 9 | |

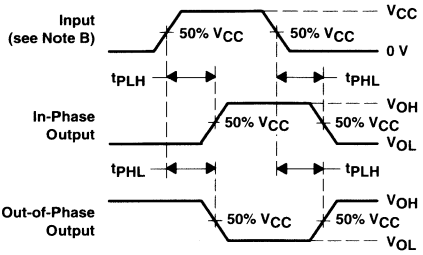
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 18 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

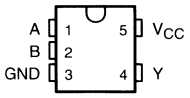
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

SCLS315D – MARCH 1996 – REVISED JUNE 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




## description

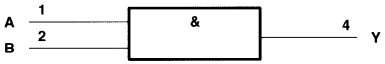
The SN74AHCT1G08 is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN74AHCT1G08 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

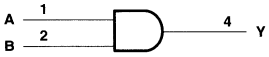
| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




EPIC is a trademark of Texas Instruments Incorporated.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

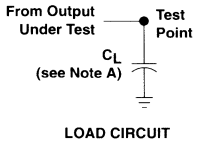
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 6.9 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9 | |

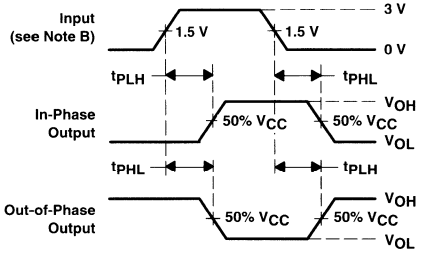
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 18 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

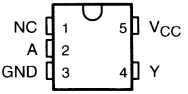
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

SCLS321D – MARCH 1996 – REVISED JUNE 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The SN74AHC1G14 contains one inverter gate. The device performs the Boolean function $Y = \overline{A}$.

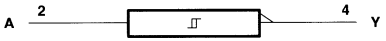
The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- ($V_{T+}$) and negative-going ($V_{T-}$) signals.

The SN74AHC1G14 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)


EPIC is a trademark of Texas Instruments Incorporated.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{T+}$ Positive-going input threshold voltage | | 3 V | | | 2.2 | | 2.2 | V |
| | | 4.5 V | | | 3.15 | | 3.15 | |
| | | 5.5 V | | | 3.85 | | 3.85 | |
| $V_{T-}$ Negative-going input threshold voltage | | 3 V | 0.9 | | | 0.9 | | V |
| | | 4.5 V | 1.35 | | | 1.35 | | |
| | | 5.5 V | 1.65 | | | 1.65 | | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | 3 V | 0.3 | | 1.2 | 0.3 | 1.2 | V |
| | | 4.5 V | 0.4 | | 1.4 | 0.4 | 1.4 | |
| | | 5.5 V | 0.5 | | 1.6 | 0.5 | 1.6 | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | 10 | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 8.3 | 12.8 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.3 | 12.8 | 1 | 15 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 10.8 | 16.3 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.8 | 16.3 | 1 | 18.5 | |

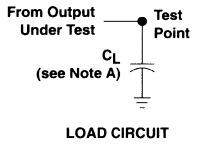
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5.5 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 5.5 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7 | 10.6 | 1 | 12 | |

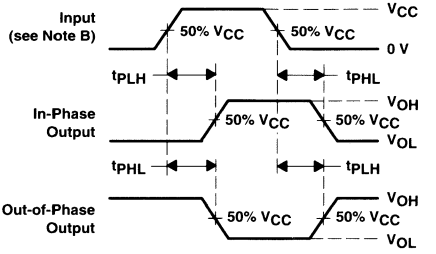
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 9 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



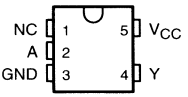

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The SN74AHCT1G14 contains a single inverter gate. The device performs the Boolean function $Y = \overline{A}$.

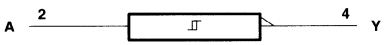
The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- ($V_{T+}$) and negative-going ($V_{T-}$) signals.

The SN74AHCT1G14 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)


EPIC is a trademark of Texas Instruments Incorporated.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.5 | V |
| $V_I$ | Input voltage | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{T+}$ Positive-going input threshold voltage | | 4.5 V | | | 2 | | 2 | V |
| | | 5.5 V | | | 2 | | 2 | |
| $V_{T-}$ Negative-going input threshold voltage | | 4.5 V | 0.5 | | | 0.5 | | V |
| | | 5.5 V | 0.6 | | | 0.6 | | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | 4.5 V | 0.4 | | 1.4 | 0.4 | 1.4 | V |
| | | 5.5 V | 0.5 | | 1.6 | 0.4 | 1.6 | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | 10 | pF |

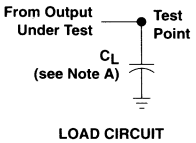
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 4 | 7 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 4 | 7 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.5 | 8 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 8 | 1 | 9 | |

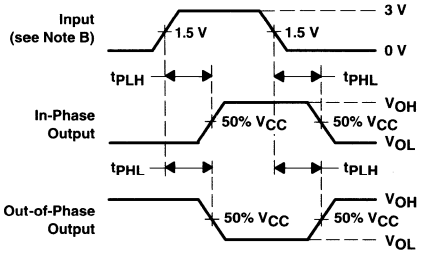
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 12 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



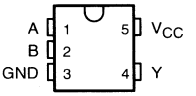

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




## description

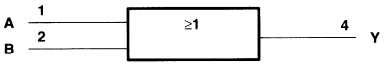
The SN74AHC1G32 is a single 2-input positive-OR gate. The device performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \bullet \overline{B}}$ in positive logic.

The SN74AHC1G32 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

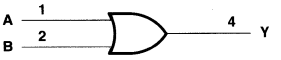
| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| H | X | H |
| X | H | H |
| L | L | L |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




EPIC is a trademark of Texas Instruments Incorporated.

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | | $I_{OH}$ = –50 µA | 2 V | 1.9 | 2 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 µA | 2 V | | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.44 | |
| $I_I$ | A or B inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | µA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | µA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | 10 | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5.5 | 7.9 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8 | 11.4 | 1 | 13 | |

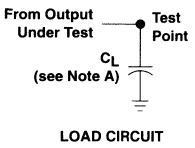
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |

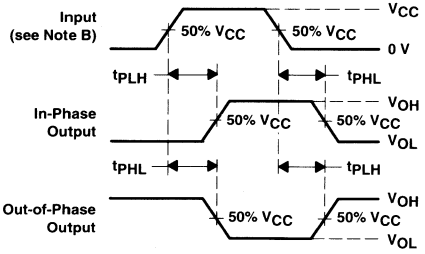
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 14 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



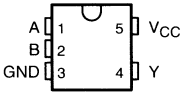

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




## description

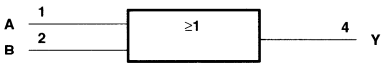
The SN74AHCT1G32 is a single 2-input positive-OR gate. The device performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \bullet \overline{B}}$ in positive logic.

The SN74AHCT1G32 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| H | X | H |
| X | H | H |
| L | L | L |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)


EPIC is a trademark of Texas Instruments Incorporated.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | | 4.5 V | 4.4 | 4.5 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | | 4.5 V | | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | | 5 V | | 2 | 10 | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

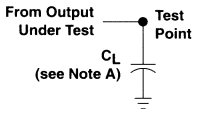
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 6.9 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9 | |

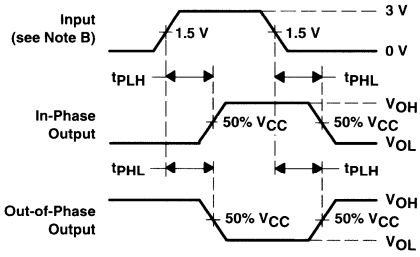
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 11.5 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

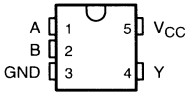
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

SCLS323D – MARCH 1996 – REVISED JUNE 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




## description

The SN74AHC1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

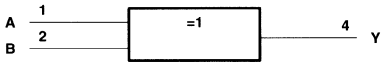
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN74AHC1G86 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

## logic symbol†

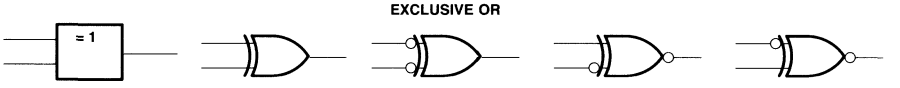



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

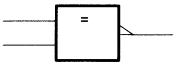
## exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



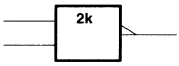

These are five equivalent exclusive-OR symbols valid for an SN74AHC1G86 gate in positive logic; negation may be shown at any two ports.

**LOGIC-IDENTITY ELEMENT**



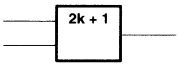

The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

**EVEN-PARITY ELEMENT**




The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

**ODD-PARITY ELEMENT**




The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$ (see Note 1) | –0.5 V to 7 V |
| Output voltage range, $V_O$ (see Note 1) | –0.5 V to $V_{CC}$ + 0.5 V |
| Input clamp current, $I_{IK}$ ($V_I$ < 0) | –20 mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) | ±20 mA |
| Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) | ±25 mA |
| Continuous current through $V_{CC}$ or GND | ±50 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 2) | 347°C/W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | | 2 V | 1.9 | 2 | | 1.9 | | V |
| | | | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | | 3 V | 2.58 | | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | | 4.5 V | 3.94 | | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | | 2 V | | | 0.1 | | 0.1 | V |
| | | | | 3 V | | | 0.1 | | 0.1 | |
| | | | | 4.5 V | | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | | 3 V | | | 0.36 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | | 4.5 V | | | 0.36 | | 0.44 | |
| $I_I$ | A or B inputs | $V_I$ = $V_{CC}$ or GND | | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | | 5 V | | 4 | 10 | | 10 | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 7 | 11 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 7 | 11 | 1 | 13 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 9.5 | 14.5 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | | 9.5 | 14.5 | 1 | 16.5 | |

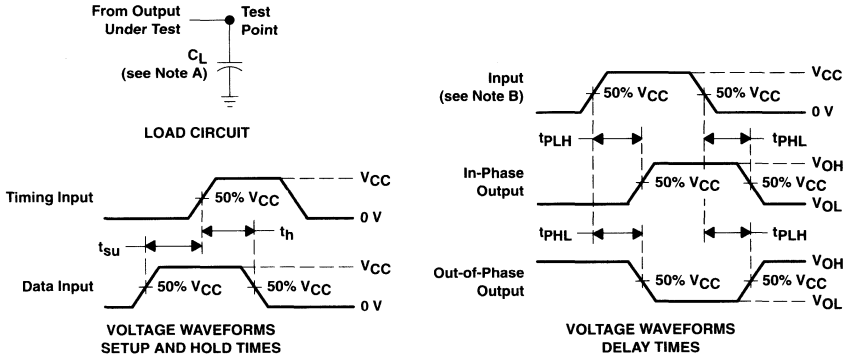
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 4.8 | 6.8 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 4.8 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 6.3 | 8.8 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 6.3 | 8.8 | 1 | 10 | |

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 18 | pF |

## PARAMETER MEASUREMENT INFORMATION



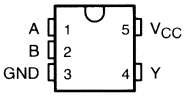

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

SCLS324D – MARCH 1996 – REVISED JUNE 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




## description

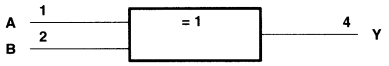
The SN74AHCT1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

The SN74AHCT1G86 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

## logic symbol†

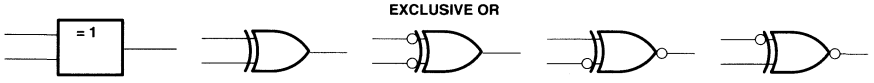



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

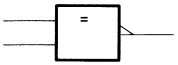
## exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



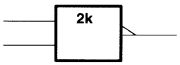

These five equivalent exclusive-OR symbols are valid for an SN74LVC86A gate in positive logic; negation may be shown at any two ports.

**LOGIC-IDENTITY ELEMENT**



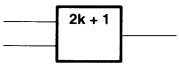

The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

**EVEN-PARITY ELEMENT**




The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

**ODD-PARITY ELEMENT**




The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at GND or $V_{CC}$ | 5.5 V | | | 1.35 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

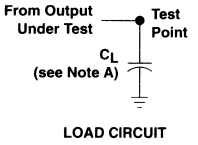
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 6.9 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9 | |

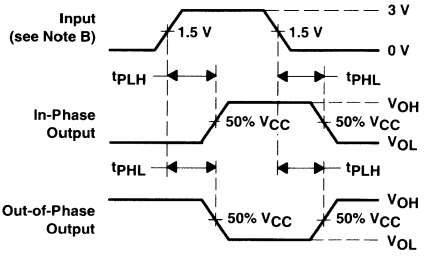
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 18 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



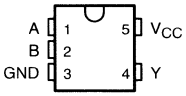

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Operation From Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Same Pinout as SN74AHC1G00**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




## description

The SN74AHC1G132 is a single NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. This device performs the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

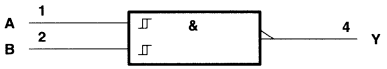
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN74AHC1G132 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

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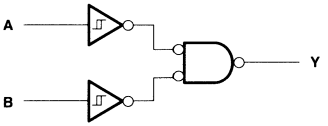
### logic diagram (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{T+}$ Positive-going input threshold voltage | | 3 V | | | 2.2 | | 2.2 | V |
| | | 4.5 V | | | 3.15 | | 3.15 | |
| | | 5.5 V | | | 3.85 | | 3.85 | |
| $V_{T-}$ Negative-going input threshold voltage | | 3 V | 0.9 | | | 0.9 | | V |
| | | 4.5 V | 1.35 | | | 1.35 | | |
| | | 5.5 V | 1.65 | | | 1.65 | | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | 3 V | 0.3 | | 1.2 | 0.3 | 1.2 | V |
| | | 4.5 V | 0.4 | | 1.4 | 0.4 | 1.4 | |
| | | 5.5 V | 0.5 | | 1.6 | 0.5 | 1.6 | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | 10 | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5.5 | 7.9 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8 | 11.4 | 1 | 13 | |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

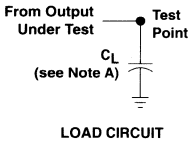
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 3.7 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.7 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.2 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.2 | 7.5 | 1 | 8.5 | |

PRODUCT PREVIEW

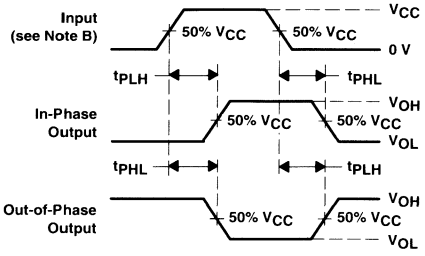
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

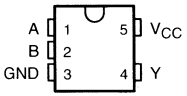
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Operation From Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Same Pinout as SN74AHCT1G00**
- **Packaged in Plastic Small-Outline Transistor Package**

**DBV PACKAGE**
**(TOP VIEW)**




## description

The SN74AHCT1G132 is a single NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. This device performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

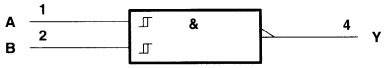
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN74AHCT1G132 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

## logic symbol†

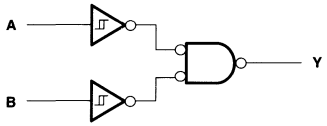



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

### logic diagram (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) ..... 347°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{T+}$ Positive-going input threshold voltage | | 4.5 V | | | 1.9 | | 1.9 | V |
| | | 5.5 V | | | 2.1 | | 2.1 | |
| $V_{T-}$ Negative-going input threshold voltage | | 4.5 V | 0.5 | | | 0.5 | | V |
| | | 5.5 V | 0.6 | | | 0.6 | | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | 4.5 V | 0.4 | | 1.4 | 0.4 | 1.4 | V |
| | | 5.5 V | 0.4 | | 1.5 | 0.4 | 1.5 | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

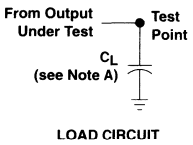
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 6.9 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9 | |

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

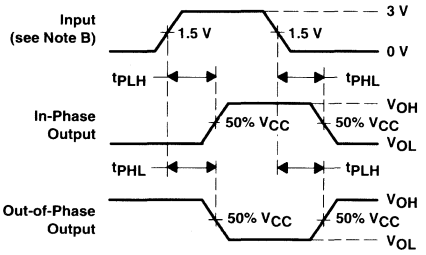
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | | pF |

PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The output is measured with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

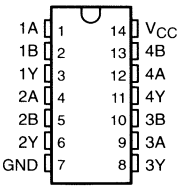
## Contents

## Contents (continued)

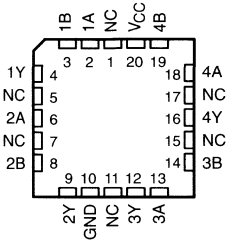
## Contents (continued)

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC00 . . . J OR W PACKAGE**
**SN74AHC00 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC00 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC00 perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

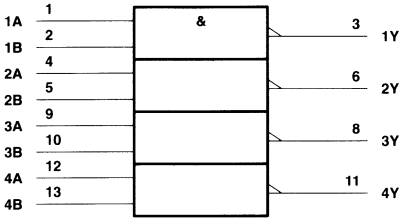
The SN54AHC00 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC00 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

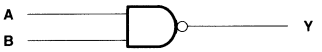
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## logic diagram, (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
DGV package ..... 182°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC00 | | SN74AHC00 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC00 | | SN74AHC00 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | A or B inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC00 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 5.5 | 7.9 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.5 | 7.9 | 1 | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8 | 11.4 | 1 | 13 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC00 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5.5 | 7.9 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8 | 11.4 | 1 | 13 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC00 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 3.7 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.7 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.2 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.2 | 7.5 | 1 | 8.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC00 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 3.7 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.7 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.2 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.2 | 7.5 | 1 | 8.5 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

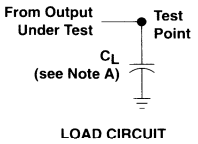
| PARAMETER | | SN74AHC00 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.3 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.3 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.6 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

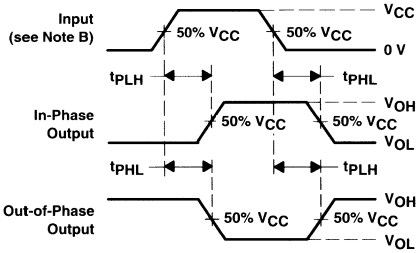
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 9.5 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



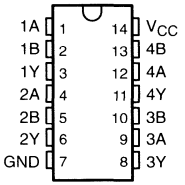

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

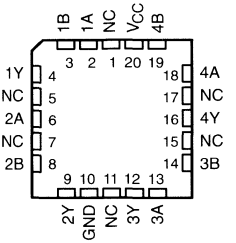
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT00 . . . J OR W PACKAGE**
**SN74AHCT00 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT00 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHCT00 perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

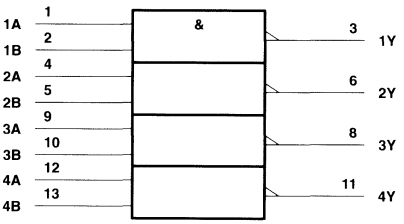
The SN54AHCT00 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT00 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| H | H | L |
| L | X | H |
| X | L | H |

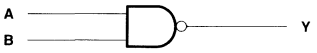
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, DGV, J, N, PW, and W packages.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
DGV package ..... 182°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT00 | | SN74AHCT00 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT00 | | SN74AHCT00 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT00 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX |
| | | | | MIN | TYP | MAX | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 | 8 | ns |
| $t_{PHL}$* | | | | | 5 | 6.9 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT00 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 6.9 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

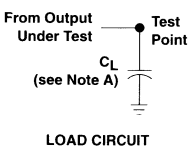
| PARAMETER | | SN74AHCT00 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.5 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

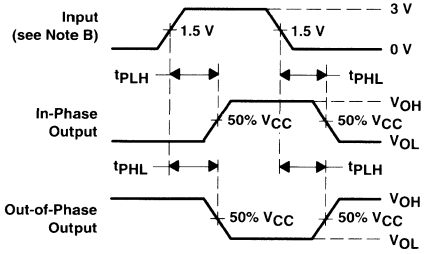
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 10.5 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



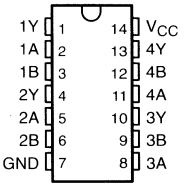

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

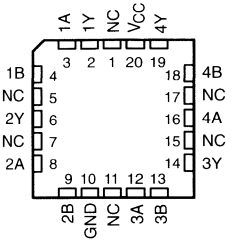
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC02 . . . J OR W PACKAGE**
**SN74AHC02 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC02 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC02 contain four independent 2-input NOR gates that perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

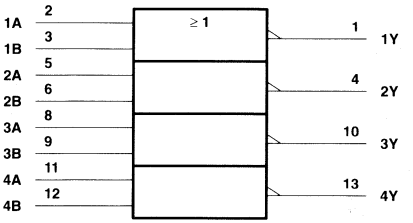
The SN54AHC02 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC02 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | X | L |
| X | H | L |
| L | L | H |

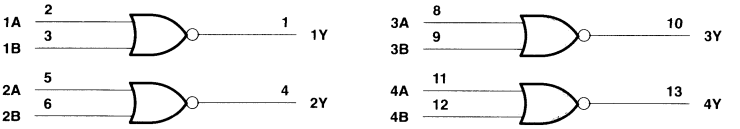
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I < 0$) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
DGV package ..... 182°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC02 | | SN74AHC02 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC02 | | SN74AHC02 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC02 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 5.6 | 7.9 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.6 | 7.9 | 1 | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.1 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.4 | 1 | 13 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC02 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5.6 | 7.9 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 7.9 | 1 | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.1 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.4 | 1 | 13 | |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC02 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 3.6 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.6 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.1 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.1 | 7.5 | 1 | 8.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC02 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 3.6 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.6 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.1 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.1 | 7.5 | 1 | 8.5 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

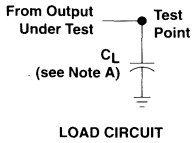
| PARAMETER | | SN74AHC02 MIN | SN74AHC02 MAX | UNIT |
|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.9 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

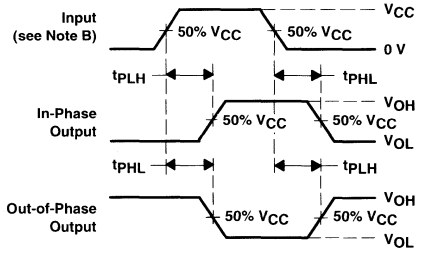
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 15 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



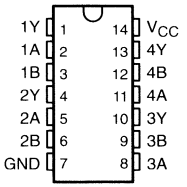

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

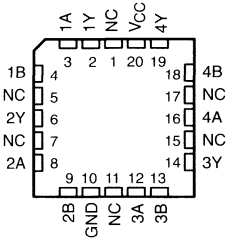
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT02 . . . J OR W PACKAGE**
**SN74AHCT02 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT02 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These devices contain four independent 2-input NOR gates that perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

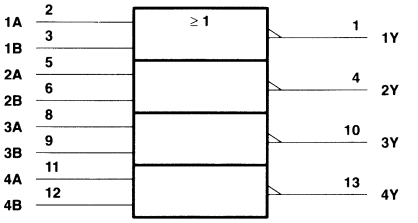
The SN54AHCT02 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT02 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | X | L |
| X | H | L |
| L | L | H |

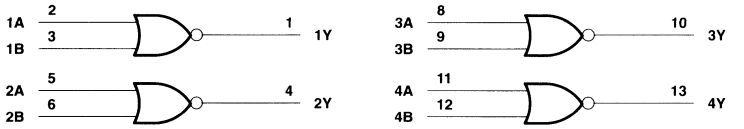
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
DGV package ..... 182°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT02 | | SN74AHCT02 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT02 | | SN74AHCT02 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at GND or $V_{CC}$ | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT02 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 2.4 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.5 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 3.4 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 4.5 | 7.5 | 1 | 8.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT02 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN MAX | |
| | | | | MIN | TYP | MAX | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 2.4 | 5.5 | 1 6.5 | ns |
| $t_{PHL}$ | | | | | 3.5 | 5.5 | 1 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 3.4 | 7.5 | 1 8.5 | ns |
| $t_{PHL}$ | | | | | 4.5 | 7.5 | 1 8.5 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

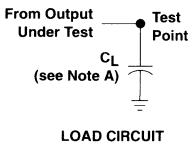
| PARAMETER | | SN74AHCT02 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.7 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

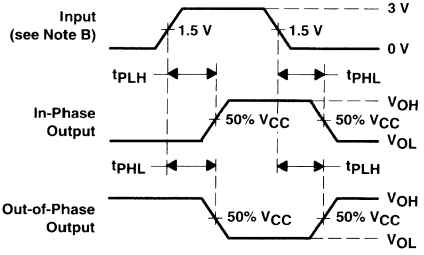
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 17 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

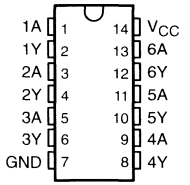
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

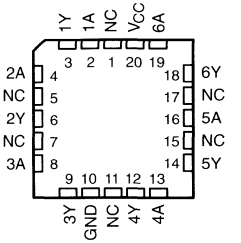
SCLS231F – OCTOBER 1995 – REVISED JUNE 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC04 . . . J OR W PACKAGE**
**SN74AHC04 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC04 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

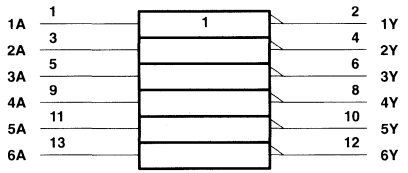
The 'AHC04 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

The SN54AHC04 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC04 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each inverter)**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

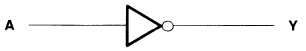
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

EPIC is a trademark of Texas Instruments Incorporated.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 127°C/W
DB package . . . . . 158°C/W
DGV package . . . . . 182°C/W
N package . . . . . 78°C/W
PW package . . . . . 170°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC04 | | SN74AHC04 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC04 | | SN74AHC04 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC04 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5 | 7.1 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5 | 7.1 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.5 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.5 | 10.6 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC04 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5 | 7.1 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5 | 7.1 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.5 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.5 | 10.6 | 1 | 12 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC04 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC04 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

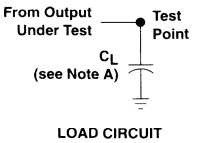
| PARAMETER | | SN74AHC04 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.8 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

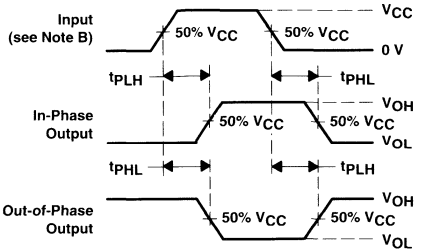
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 12 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



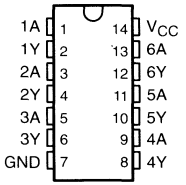

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

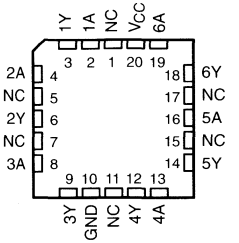
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Unbuffered Outputs**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCU04 . . . J OR W PACKAGE**
**SN74AHCU04 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCU04 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHCU04 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$. Internal circuitry consists of single-stage inverters that can be used in analog applications such as crystal oscillators.

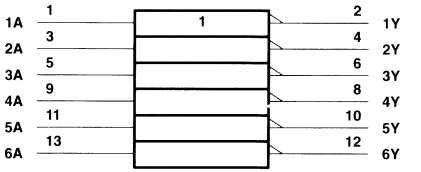
The SN54AHCU04 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCU04 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each inverter)**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

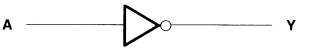
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
DGV package ..... 182°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHCU04 | | SN74AHCU04 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.7 | | 1.7 | | V |
| | | $V_{CC}$ = 3 V | 2.4 | | 2.4 | | |
| | | $V_{CC}$ = 5.5 V | 4.4 | | 4.4 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.3 | | 0.3 | V |
| | | $V_{CC}$ = 3 V | | 0.6 | | 0.6 | |
| | | $V_{CC}$ = 5.5 V | | 1.1 | | 1.1 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCU04 | | SN74AHCU04 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.8 | 2 | | 1.8 | | 1.8 | | V |
| | | 3 V | 2.7 | 3 | | 2.7 | | 2.7 | | |
| | | 4.5 V | 4 | 4.5 | | 4 | | 4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.2 | | 0.2 | | 0.2 | V |
| | | 3 V | | | 0.3 | | 0.3 | | 0.3 | |
| | | 4.5 V | | | 0.5 | | 0.5 | | 0.5 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCU04 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5 | 8.9 | 1 | 10.5 | ns |
| $t_{PHL}$* | | | | | 5 | 8.9 | 1 | 10.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.5 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 7.5 | 11.4 | 1 | 13 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCU04 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5 | 8.9 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5 | 8.9 | 1 | 10.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.5 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 7.5 | 11.4 | 1 | 13 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCU04 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.5 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.5 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5 | 7 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 7 | 1 | 8 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCU04 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.5 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.5 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5 | 7 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 7 | 1 | 8 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

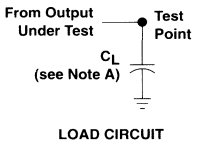
| PARAMETER | | SN74AHCU04 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.5 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.5 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.3 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 4 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

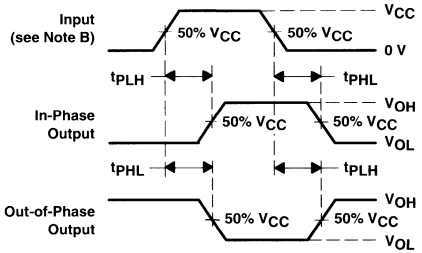
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 7.3 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



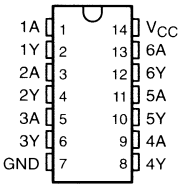

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

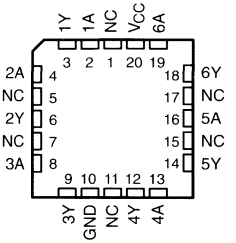
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT04 . . . J OR W PACKAGE**
**SN74AHCT04 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT04 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

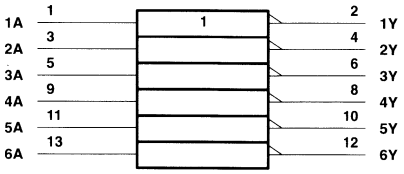
The 'AHCT04 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

The SN54AHCT04 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT04 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each inverter)**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

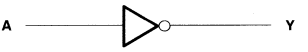
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

EPIC is a trademark of Texas Instruments Incorporated.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
DGV package ..... 182°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT04 | | SN74AHCT04 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT04 | | SN74AHCT04 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT04 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN MAX | |
| | | | | MIN | TYP | MAX | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 4.7 | 6.7 | 1 7.5 | ns |
| $t_{PHL}$* | | | | | 4.7 | 6.7 | 1 7.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.5 | 7.7 | 1 8.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.7 | 1 8.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT04 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN MAX | |
| | | | | MIN | TYP | MAX | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 4.7 | 6.7 | 1 7.5 | ns |
| $t_{PHL}$ | | | | | 4.7 | 6.7 | 1 7.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.5 | 7.7 | 1 8.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.7 | 1 8.5 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

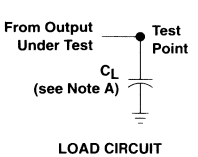
| PARAMETER | | SN74AHCT04 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.7 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

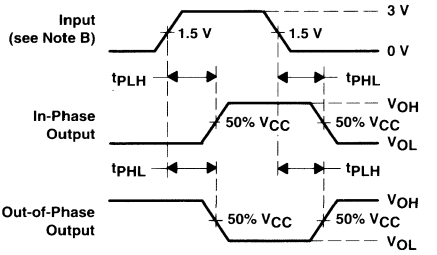
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 14 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



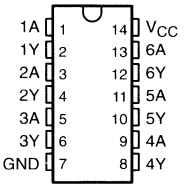

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

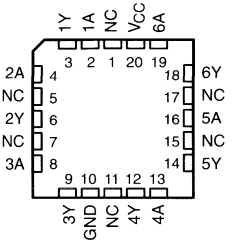
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC05 . . . J OR W PACKAGE**
**SN74AHC05 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC05 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

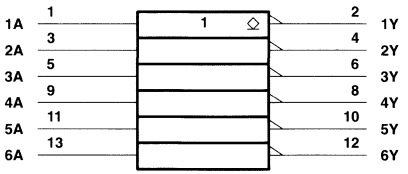
The 'AHC05 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$. The open-drain outputs require pullup resistors to perform correctly. They can be connected to other open-drain outputs to implement acitve-low wired-OR or active-high wired-AND functions.

The SN54AHC05 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC05 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each inverter)**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

## logic symbol†

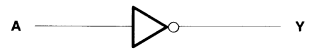



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

### logic diagram (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | | SN54AHC05 | | SN74AHC05 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC05 | | SN74AHC05 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $I_{OH}$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | 0.01 | 0.5 | | 10 | | 5 | μA |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC05 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5 | 7.1 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5 | 7.1 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.5 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.5 | 10.6 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC05 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5 | 7.1 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5 | 7.1 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.5 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.5 | 10.6 | 1 | 12 | |

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC05 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC05 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

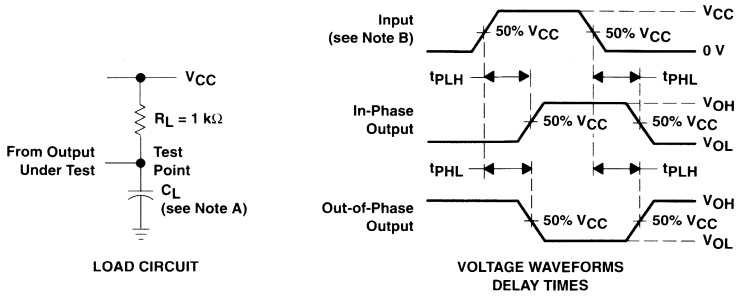
| PARAMETER | | SN74AHC05 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.8 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 12 | pF |

## PARAMETER MEASUREMENT INFORMATION



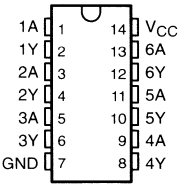

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

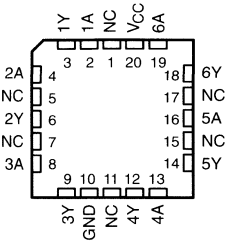
PRODUCT PREVIEW

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT05 . . . J OR W PACKAGE**
**SN74AHCT05 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT05 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

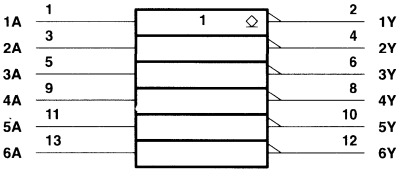
The 'AHCT05 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$. The open-drain outputs require pullup resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The SN54AHCT05 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT05 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each inverter)**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

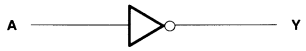
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

EPIC is a trademark of Texas Instruments Incorporated.

### logic diagram (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 127°C/W
DB package . . . . . 158°C/W
N package . . . . . 78°C/W
PW package . . . . . 170°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | SN54AHCT05 | | SN74AHCT05 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT05 | | SN74AHCT05 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT05 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT05 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

| PARAMETER | | SN74AHCT05 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.8 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

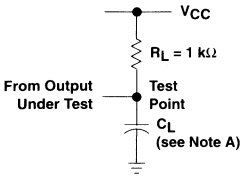
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

PRODUCT PREVIEW

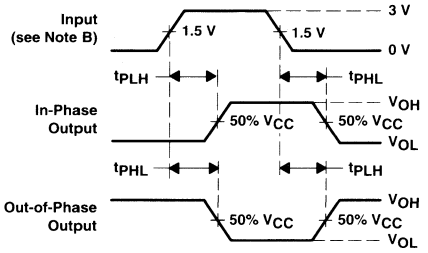
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 12 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

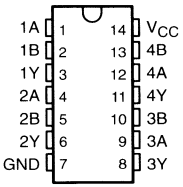
NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

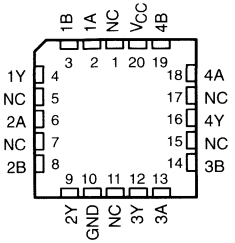
PRODUCT PREVIEW

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC08 . . . J OR W PACKAGE**
**SN74AHC08 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC08 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC08 are quadruple 2-input positive-AND gates. These devices perform the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

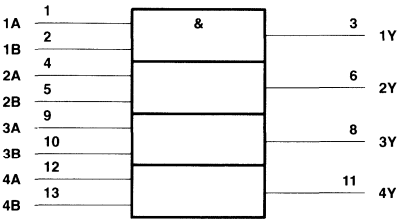
The SN54AHC08 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC08 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

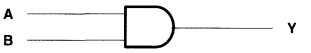
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stressratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC08 | | SN74AHC08 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC08 | | SN74AHC08 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | A or B inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC08 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 6.2 | 8.8 | 1 | 10.5 | ns |
| $t_{PHL}$* | | | | | 6.2 | 8.8 | 1 | 10.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 8.7 | 12.3 | 1 | 14 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC08 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 6.2 | 8.8 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.2 | 8.8 | 1 | 10.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 8.7 | 12.3 | 1 | 14 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC08 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 4.3 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$* | | | | | 4.3 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.8 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.8 | 7.9 | 1 | 9 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC08 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 4.3 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$ | | | | | 4.3 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.8 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.8 | 7.9 | 1 | 9 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

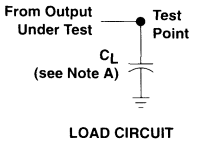
| PARAMETER | | SN74AHC08 MIN | SN74AHC08 MAX | UNIT |
|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

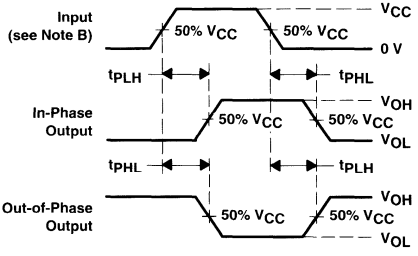
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 18 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

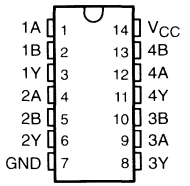
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

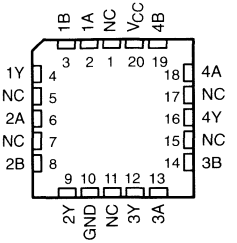
SCLS237D – OCTOBER 1995 – REVISED JUNE 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT08 . . . J OR W PACKAGE**
**SN74AHCT08 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT08 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHCT08 are quadruple 2-input positive-AND gates. These devices perform the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

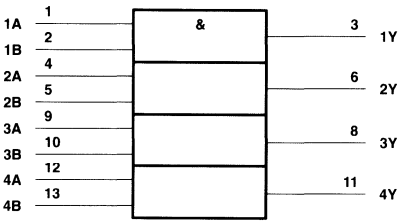
The SN54AHCT08 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT08 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## logic diagram (positive logic)


## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I < 0$) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
DGV package ..... 182°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT08 | | SN74AHCT08 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT08 | | SN74AHCT08 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT08 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN MAX | |
| | | | | MIN | TYP | MAX | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 8 | ns |
| $t_{PHL}$* | | | | | 5 | 6.9 | 1 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 9 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT08 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN MAX | |
| | | | | MIN | TYP | MAX | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 8 | ns |
| $t_{PHL}$ | | | | | 5 | 6.9 | 1 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 9 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

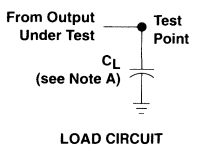
| PARAMETER | | SN74AHCT08 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.4 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

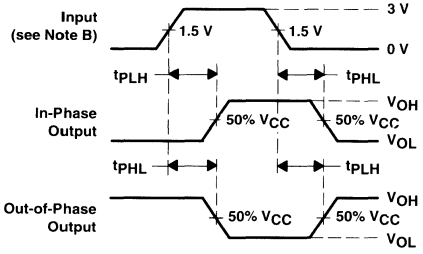
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 18 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

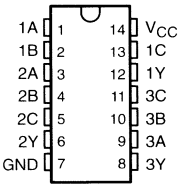
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

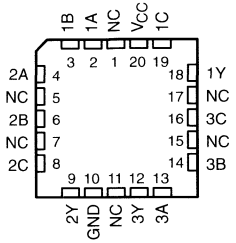
SCLS359 – MAY 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC10 . . . J OR W PACKAGE**
**SN74AHC10 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC10 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

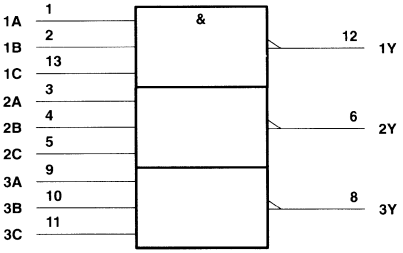
These devices contain three independent 3-input NAND gates. They perform the Boolean function $Y = \overline{A \bullet B \bullet C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54AHC10 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC10 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | H | H | L |
| L | X | X | H |
| X | L | X | H |
| X | X | L | H |

## logic symbol†

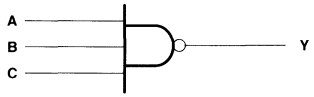



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

### logic diagram, each gate (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | | SN54AHC10 | | SN74AHC10 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC10 | | SN74AHC10 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC10 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A, B, or C | Y | $C_L$ = 15 pF | | 5.7 | 8.4 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 5.7 | 8.4 | 1 | 10 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 8.2 | 11.9 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 8.2 | 11.9 | 1 | 13.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC10 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 15 pF | | 5.7 | 8.4 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 5.7 | 8.4 | 1 | 10 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 8.2 | 11.9 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 8.2 | 11.9 | 1 | 13.5 | |

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC10 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A, B, or C | Y | $C_L$ = 15 pF | | 3.9 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$* | | | | | 3.9 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.4 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.4 | 7.9 | 1 | 9 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC10 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 15 pF | | 3.9 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$ | | | | | 3.9 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.4 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.4 | 7.9 | 1 | 9 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

| PARAMETER | | SN74AHC10 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

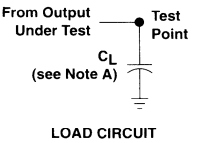
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

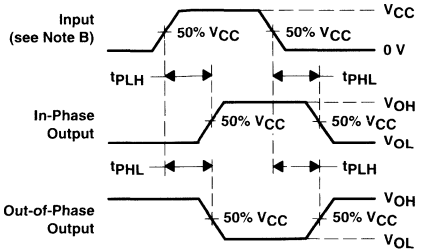
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 14 | pF |

PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

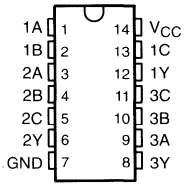
**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

SCLS360 – MAY 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT10 . . . J OR W PACKAGE**
**SN74AHCT10 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




## description

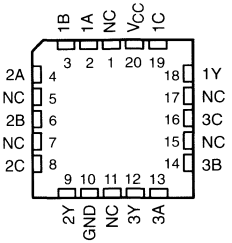
These devices contain three independent 3-input NAND gates. They perform the Boolean function $Y = \overline{A \bullet B \bullet C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54AHCT10 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT10 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

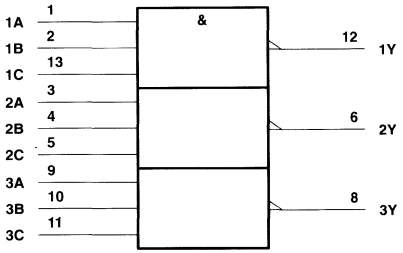
| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | H | H | L |
| L | X | X | H |
| X | L | X | H |
| X | X | L | H |

**SN54AHCT10 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

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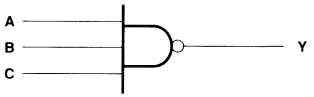
### logic diagram, each gate (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | SN54AHCT10 | | SN74AHCT10 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT10 | | SN74AHCT10 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT10 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN MAX | |
| | | | | MIN | TYP | MAX | | |
| $t_{PLH}$* | A, B, or C | Y | $C_L$ = 15 pF | | 3.9 | 5.9 | 1 7 | ns |
| $t_{PHL}$* | | | | | 3.9 | 5.9 | 1 7 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.4 | 7.9 | 1 9 | ns |
| $t_{PHL}$ | | | | | 5.4 | 7.9 | 1 9 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT10 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN MAX | |
| | | | | MIN | TYP | MAX | | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 15 pF | | 3.9 | 5.9 | 1 7 | ns |
| $t_{PHL}$ | | | | | 3.9 | 5.9 | 1 7 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.4 | 7.9 | 1 9 | ns |
| $t_{PHL}$ | | | | | 5.4 | 7.9 | 1 9 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

| PARAMETER | | SN74AHCT10 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

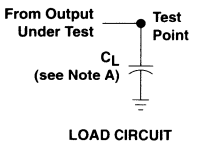
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

PRODUCT PREVIEW

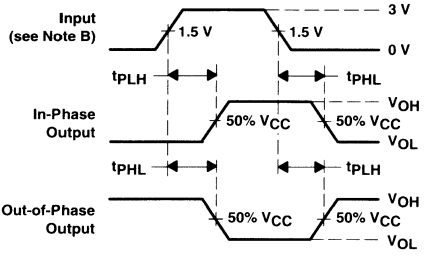
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 14 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

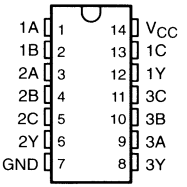
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

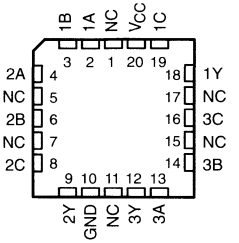
SCLS361 – MAY 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC11 . . . J OR W PACKAGE**
**SN74AHC11 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC11 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

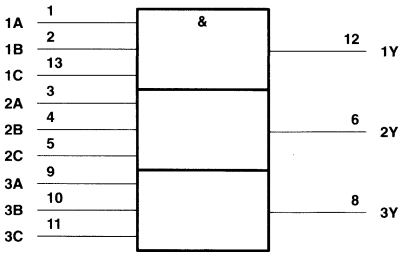
These devices contain three independent 3-input AND gates. They perform the Boolean function $Y = A \bullet B \bullet C$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$ in positive logic.

The SN54AHC11 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC11 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | H | H | H |
| L | X | X | L |
| X | L | X | L |
| X | X | L | L |

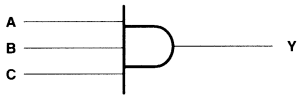
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

EPIC is a trademark of Texas Instruments Incorporated.

## logic diagram, each gate (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC11 | | SN74AHC11 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC11 | | SN74AHC11 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC11 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A, B, or C | Y | $C_L$ = 15 pF | | 6.1 | 8.8 | 1 | 10.5 | ns |
| $t_{PHL}$* | | | | | 6.1 | 8.8 | 1 | 10.5 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 8.6 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 8.6 | 12.3 | 1 | 14 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC11 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 15 pF | | 6.1 | 8.8 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.1 | 8.8 | 1 | 10.5 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 8.6 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 8.6 | 12.3 | 1 | 14 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC11 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A, B, or C | Y | $C_L$ = 15 pF | | 4.1 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$* | | | | | 4.1 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.6 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.6 | 7.9 | 1 | 9 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC11 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 15 pF | | 4.1 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$ | | | | | 4.1 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.6 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.6 | 7.9 | 1 | 9 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

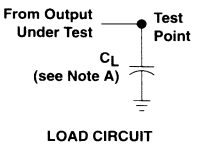
| PARAMETER | | SN74AHC11 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

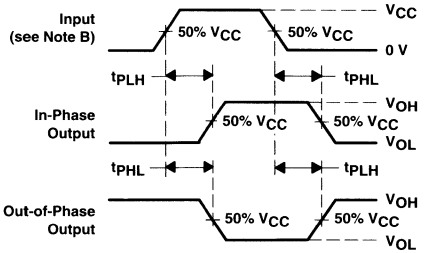
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 17 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

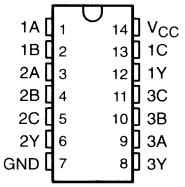
**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

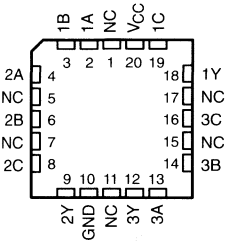
SCLS362 – MAY 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT11 . . . J OR W PACKAGE**
**SN74AHCT11 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT11 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

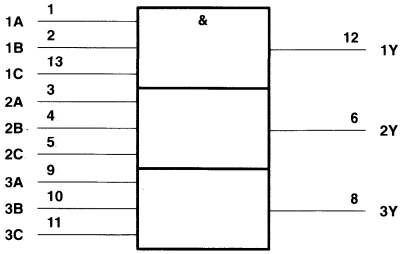
These devices contain three independent 3-input AND gates. They perform the Boolean function $Y = A \bullet B \bullet C$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$ in positive logic.

The SN54AHCT11 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT11 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | H | H | H |
| L | X | X | L |
| X | L | X | L |
| X | X | L | L |

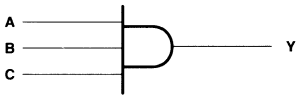
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

EPIC is a trademark of Texas Instruments Incorporated.

### logic diagram, each gate (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | SN54AHCT11 | | SN74AHCT11 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT11 | | SN74AHCT11 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT11 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A, B, or C | Y | $C_L$ = 15 pF | | 4.1 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$* | | | | | 4.1 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.6 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.6 | 7.9 | 1 | 9 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT11 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 15 pF | | 4.1 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$ | | | | | 4.1 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.6 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.6 | 7.9 | 1 | 9 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

| PARAMETER | | SN74AHCT11 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

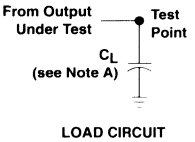
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

PRODUCT PREVIEW

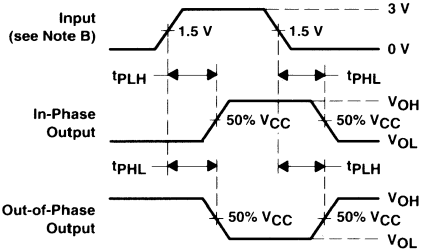
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 17 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

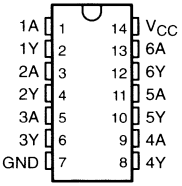
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

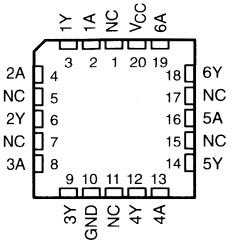
SCLS238C – OCTOBER 1995 – REVISED MAY 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC14 . . . J OR W PACKAGE**
**SN74AHC14 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC14 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC14 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going ($V_{T+}$) and negative-going ($V_{T-}$) signals.

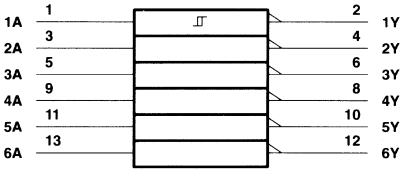
The SN54AHC14 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC14 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

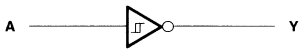
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 127°C/W
DB package . . . . . 158°C/W
N package . . . . . 78°C/W
PW package . . . . . 170°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC14 | | SN74AHC14 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC14 | | SN74AHC14 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{T+}$ Positive-going input threshold voltage | | 3 V | | | 2.2 | | 2.2 | | 2.2 | V |
| | | 4.5 V | | | 3.15 | | 3.15 | | 3.15 | |
| | | 5.5 V | | | 3.85 | | 3.85 | | 3.85 | |
| $V_{T-}$ Negative-going input threshold voltage | | 3 V | 0.9 | | | 0.9 | | 0.9 | | V |
| | | 4.5 V | 1.35 | | | 1.35 | | 1.35 | | |
| | | 5.5 V | 1.65 | | | 1.65 | | 1.65 | | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | 3 V | 0.3 | | 1.2 | 0.3 | 1.2 | 0.3 | 1.2 | V |
| | | 4.5 V | 0.4 | | 1.4 | 0.4 | 1.4 | 0.4 | 1.4 | |
| | | 5.5 V | 0.5 | | 1.6 | 0.5 | 1.6 | 0.5 | 1.6 | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC14 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 8.3 | 12.8 | 1 | 15 | ns |
| $t_{PHL}$* | | | | | 8.3 | 12.8 | 1 | 15 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 10.8 | 16.3 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.8 | 16.3 | 1 | 18.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC14 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 8.3 | 12.8 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.3 | 12.8 | 1 | 15 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 10.8 | 16.3 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.8 | 16.3 | 1 | 18.5 | |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC14 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5.5 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 5.5 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7 | 10.6 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC14 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5.5 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 5.5 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7 | 10.6 | 1 | 12 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

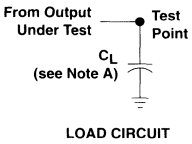
| PARAMETER | | SN74AHC14 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.6 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

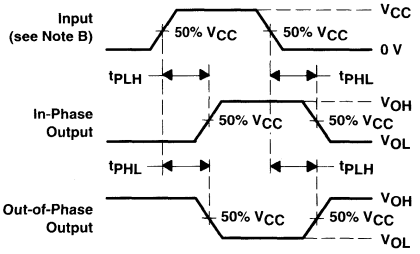
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 9 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



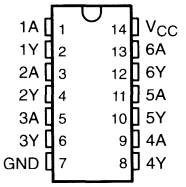

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

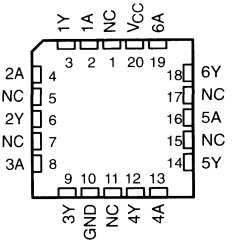
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT14 . . . J OR W PACKAGE**
**SN74AHCT14 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT14 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHCT14 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going ($V_{T+}$) and for negative-going ($V_{T-}$) signals.

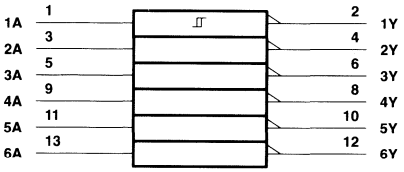
The SN54AHCT14 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT14 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each inverter)**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

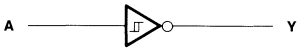
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
DGV package ..... 182°C/W
N package ..... 76°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT14 | | SN74AHCT14 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2.1 | | 2.1 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.5 | | 0.5 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT14 | | SN74AHCT14 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{T+}$ Positive-going input threshold voltage | | 4.5 V | | | 1.9 | | 1.9 | | 1.9 | V |
| | | 5.5 V | | | 2.1 | | 2.1 | | 2.1 | |
| $V_{T-}$ Negative-going input threshold voltage | | 4.5 V | 0.5 | | | 0.5 | | 0.5 | | V |
| | | 5.5 V | 0.6 | | | 0.6 | | 0.6 | | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | 4.5 V | 0.4 | | 1.4 | 0.4 | 1.4 | 0.4 | 1.4 | V |
| | | 5.5 V | 0.4 | | 1.5 | 0.4 | 1.5 | 0.4 | 1.5 | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT14 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | | 4 | 7 | 1 | 8 | ns |
| $t_{PHL}$* | | | | | | 4 | 7 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | | 5.5 | 8 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | | 5.5 | 8 | 1 | 9 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT14 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 4 | 7 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 4 | 7 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.5 | 8 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 8 | 1 | 9 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

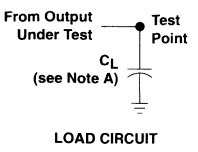
| PARAMETER | | SN74AHCT14 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.9 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.7 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.3 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.1 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

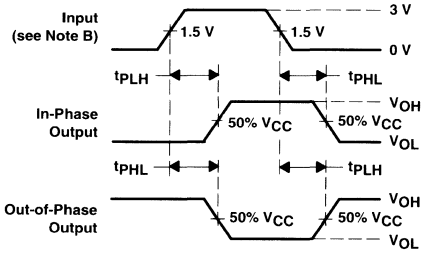
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 12 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

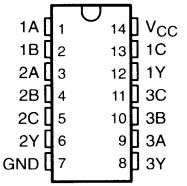
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

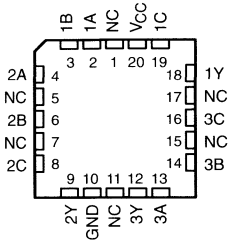
SCLS363 – MAY 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC27 . . . J OR W PACKAGE**
**SN74AHC27 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC27 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

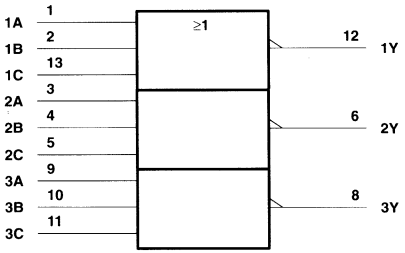
These devices contain three independent 3-input NOR gates. They perform the Boolean function $Y = \overline{A} + \overline{B} + \overline{C}$ or $Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$ in positive logic.

The SN54AHC27 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC27 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | X | X | L |
| X | H | X | L |
| X | X | H | L |
| L | L | L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

## logic diagram, each gate (positive logic)


## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC27 | | SN74AHC27 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC27 | | SN74AHC27 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC27 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A, B, or C | Y | $C_L$ = 15 pF | | 6.2 | 8.8 | 1 | 10.5 | ns |
| $t_{PHL}$* | | | | | 6.2 | 8.8 | 1 | 10.5 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 8.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 8.7 | 12.3 | 1 | 14 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC27 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 15 pF | | 6.2 | 8.8 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.2 | 8.8 | 1 | 10.5 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 8.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 8.7 | 12.3 | 1 | 14 | |

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC27 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A, B, or C | Y | $C_L$ = 15 pF | | 4.1 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$* | | | | | 4.1 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.6 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.6 | 7.9 | 1 | 9 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC27 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 15 pF | | 4.1 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$ | | | | | 4.1 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.6 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.6 | 7.9 | 1 | 9 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

| PARAMETER | | SN74AHC27 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

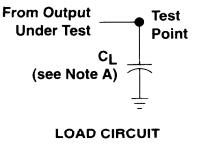
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

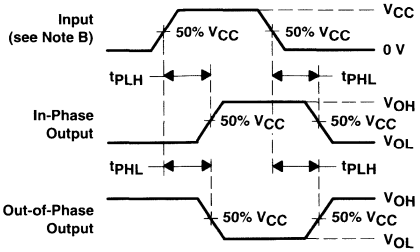
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 14 | pF |

PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

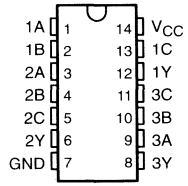
**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

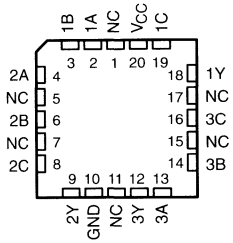
SCLS364 – MAY 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT27 . . . J OR W PACKAGE**
**SN74AHCT27 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT27 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

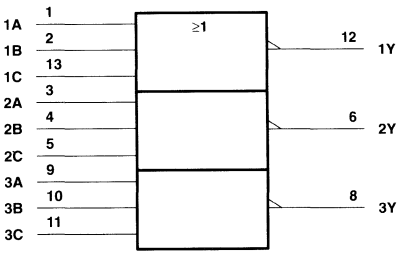
These devices contain three independent 3-input NOR gates. They perform the Boolean function $Y = \overline{A + B + C}$ or $Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$ in positive logic.

The SN54AHCT27 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT27 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | X | X | L |
| X | H | X | L |
| X | X | H | L |
| L | L | L | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

## logic diagram, each gate (positive logic)


## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT27 | | SN74AHCT27 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT27 | | SN74AHCT27 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT27 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A, B, or C | Y | $C_L$ = 15 pF | | 4.1 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$* | | | | | 4.1 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.6 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.6 | 7.9 | 1 | 9 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT27 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 15 pF | | 4.1 | 5.9 | 1 | 7 | ns |
| $t_{PHL}$ | | | | | 4.1 | 5.9 | 1 | 7 | |
| $t_{PLH}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.6 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.6 | 7.9 | 1 | 9 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

| PARAMETER | | SN74AHCT27 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

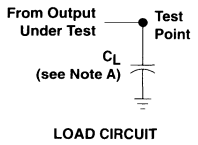
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

PRODUCT PREVIEW

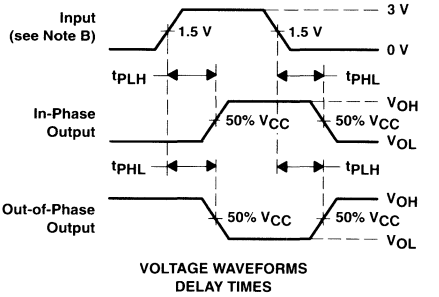
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 20 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

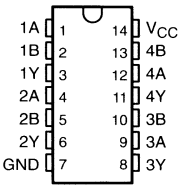
**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

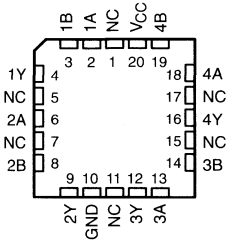
SCLS247B – OCTOBER 1995 – REVISED MAY 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC32 . . . J OR W PACKAGE**
**SN74AHC32 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC32 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC32 are quadruple 2-input positive-OR gates. These devices perform the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = A + B$ in positive logic.

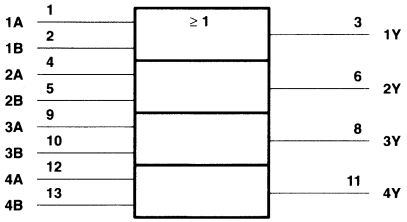
The SN54AHC32 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC32 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |

EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)


## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stressratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC32 | | SN74AHC32 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC32 | | SN74AHC32 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | A or B inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC32 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 5.5 | 7.9 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.5 | 7.9 | 1 | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8 | 11.4 | 1 | 13 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC32 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5.5 | 7.9 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8 | 11.4 | 1 | 13 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC32 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC32 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

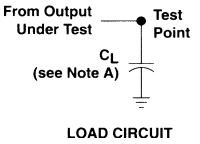
| PARAMETER | | SN74AHC32 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.3 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.3 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.7 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

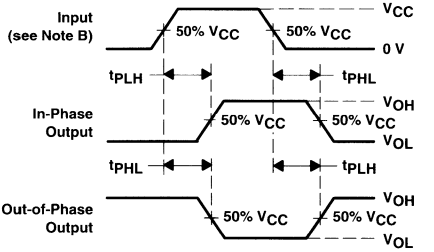
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 14 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

SCLS248D – OCTOBER 1995 – REVISED JUNE 1997

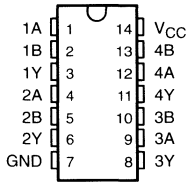
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

## description

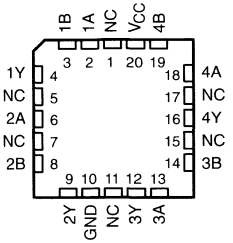
The 'AHCT32 are quadruple 2-input positive-OR gates. These devices perform the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = A + B$ in positive logic.

The SN54AHCT32 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT32 is characterized for operation from –40°C to 85°C.

**SN54AHCT32 . . . J OR W PACKAGE**
**SN74AHCT32 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT32 . . . FK PACKAGE**
**(TOP VIEW)**



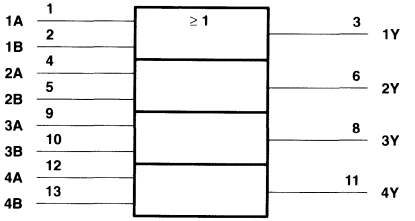

NC – No internal connection

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |

EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DGV, DW, J, N, PW, and W packages.

## logic diagram (positive logic)


## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
DGV package ..... 182°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT32 | | SN74AHCT32 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT32 | | SN74AHCT32 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT32 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX |
| | | | | MIN | TYP | MAX | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 | 8 | ns |
| $t_{PHL}$* | | | | | 5 | 6.9 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT32 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 6.9 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

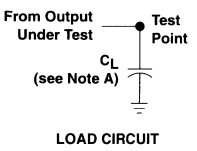
| PARAMETER | | SN74AHCT32 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.5 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

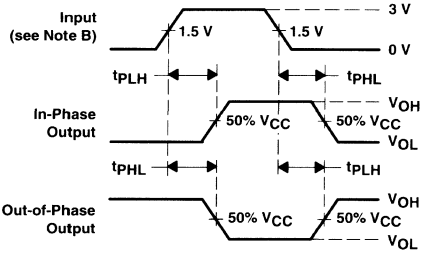
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 11.5 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



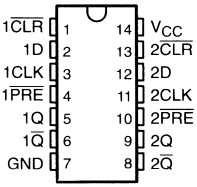

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

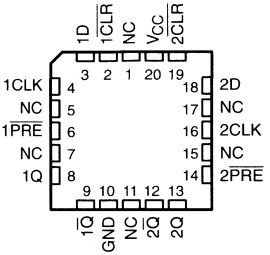
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC74 . . . J OR W PACKAGE**
**SN74AHC74 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC74 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC74 are dual positive-edge-triggered D-type flip-flops.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54AHC74 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC74 is characterized for operation from –40°C to 85°C.

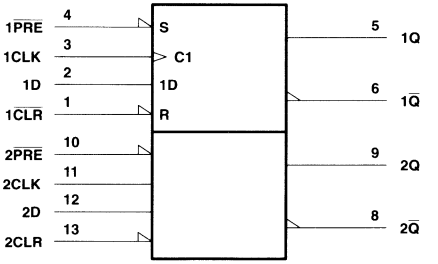
**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H† | H† |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

† This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

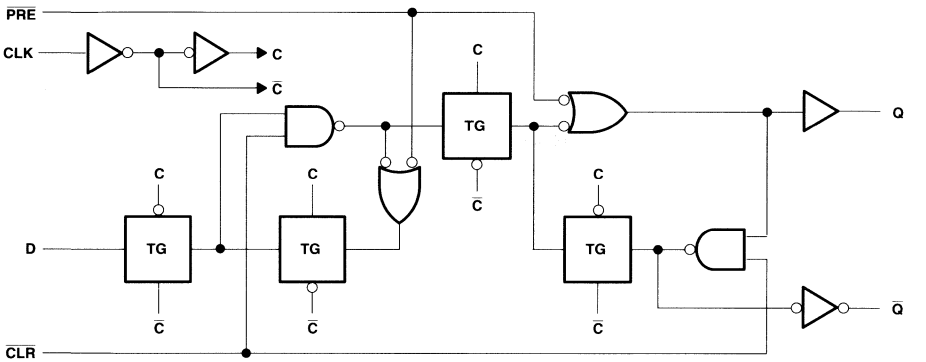
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram, each flip-flop (positive logic)



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 127°C/W
DB package . . . . . 158°C/W
N package . . . . . 78°C/W
PW package . . . . . 170°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | | SN54AHC74 | | SN74AHC74 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC74 | | SN74AHC74 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | Data inputs | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| | Control inputs | | | | | ±0.1 | | ±1 | | ±1 | |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHC74 | | SN74AHC74 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | PRE or CLR low | 6 | | 7 | | 7 | | ns |
| | | CLK | 6 | | 7 | | 7 | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 6 | | 7 | | 7 | | ns |
| | | PRE or CLR inactive | 5 | | 5 | | 5 | | |
| $t_h$ | Hold time, data after CLK↑ | | 0.5 | | 0.5 | | 0.5 | | ns |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHC74 | | SN74AHC74 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 5 | | 5 | | 5 | | ns |
| | | CLK | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 5 | | 5 | | 5 | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | 3 | | 3 | | 3 | | |
| $t_h$ | Hold time, data after CLK↑ | | 0.5 | | 0.5 | | 0.5 | | ns |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC74 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 80 | 125 | | 70 | | MHz |
| | | | $C_L$ = 50 pF | 50 | 75 | | 45 | | |
| $t_{PLH}$* | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 7.6 | 12.3 | 1 | 14.5 | ns |
| $t_{PHL}$* | | | | | 7.6 | 12.3 | 1 | 14.5 | |
| $t_{PLH}$* | CLK | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 6.7 | 11.9 | 1 | 14 | ns |
| $t_{PHL}$* | | | | | 6.7 | 11.9 | 1 | 14 | |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 10.1 | 15.8 | 1 | 18 | ns |
| $t_{PHL}$ | | | | | 10.1 | 15.8 | 1 | 18 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 9.2 | 15.4 | 1 | 17.5 | ns |
| $t_{PHL}$ | | | | | 9.2 | 15.4 | 1 | 17.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC74 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 80 | 125 | | 70 | | MHz |
| | | | $C_L$ = 50 pF | 50 | 75 | | 45 | | |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 7.6 | 12.3 | 1 | 14.5 | ns |
| $t_{PHL}$ | | | | | 7.6 | 12.3 | 1 | 14.5 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 6.7 | 11.9 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 6.7 | 11.9 | 1 | 14 | |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 10.1 | 15.8 | 1 | 18 | ns |
| $t_{PHL}$ | | | | | 10.1 | 15.8 | 1 | 18 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 9.2 | 15.4 | 1 | 17.5 | ns |
| $t_{PHL}$ | | | | | 9.2 | 15.4 | 1 | 17.5 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC74 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 130 | 170 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 90 | 115 | | 75 | | |
| $t_{PLH}$* | PRE or CLR | Q or Q | $C_L$ = 15 pF | | 4.8 | 7.7 | 1 | 9 | ns |
| $t_{PHL}$* | | | | | 4.8 | 7.7 | 1 | 9 | |
| $t_{PLH}$* | CLK | Q or Q | $C_L$ = 15 pF | | 4.6 | 7.3 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 4.6 | 7.3 | 1 | 8.5 | |
| $t_{PLH}$ | PRE or CLR | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 6.3 | 9.7 | 1 | 11 | ns |
| $t_{PHL}$ | | | | | 6.3 | 9.7 | 1 | 11 | |
| $t_{PLH}$ | CLK | Q or Q | $C_L$ = 50 pF | | 6.1 | 9.3 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.1 | 9.3 | 1 | 10.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC74 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 130 | 170 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 90 | 115 | | 75 | | |
| $t_{PLH}$ | PRE or CLR | Q or Q | $C_L$ = 15 pF | | 4.8 | 7.7 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 4.8 | 7.7 | 1 | 9 | |
| $t_{PLH}$ | CLK | Q or Q | $C_L$ = 15 pF | | 4.6 | 7.3 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 4.6 | 7.3 | 1 | 8.5 | |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 6.3 | 9.7 | 1 | 11 | ns |
| $t_{PHL}$ | | | | | 6.3 | 9.7 | 1 | 11 | |
| $t_{PLH}$ | CLK | Q or Q | $C_L$ = 50 pF | | 6.1 | 9.3 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.1 | 9.3 | 1 | 10.5 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

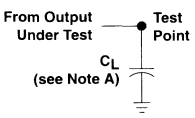
| PARAMETER | | SN74AHC74 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | 4.7 | –0.8 | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

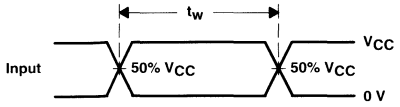
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 32 | pF |

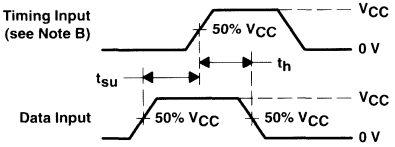
## PARAMETER MEASUREMENT INFORMATION



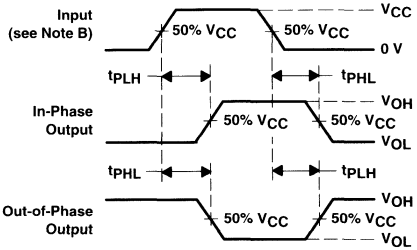

LOAD CIRCUIT




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



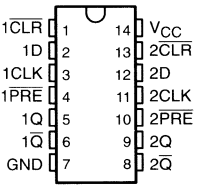

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

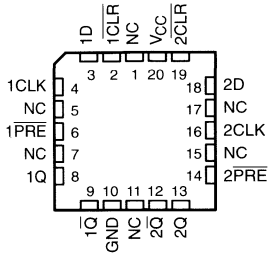
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT74 . . . J OR W PACKAGE**
**SN74AHCT74 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT74 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHCT74 are dual positive-edge-triggered D-type flip-flops.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54AHCT74 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT74 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

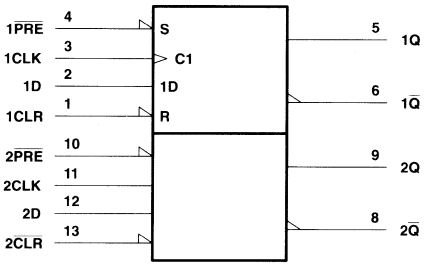
| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H† | H† |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

† This configuration is unstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

ADVANCE INFORMATION

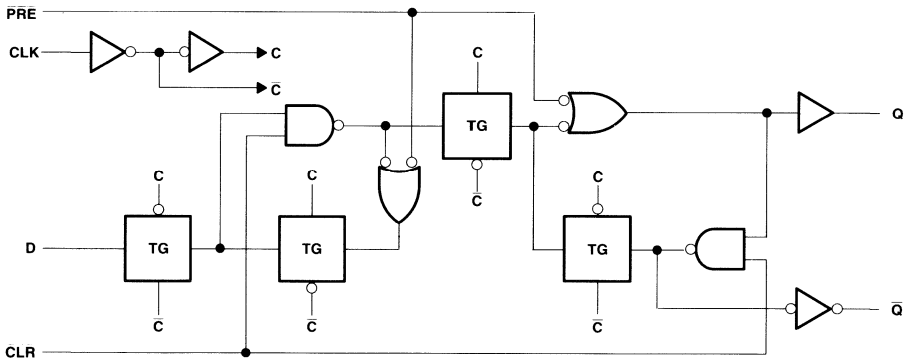
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram, each flip-flop (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | SN54AHCT74 | | SN74AHCT74 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT74 | | SN74AHCT74 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

ADVANCE INFORMATION

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

| PARAMETER | | | $T_A$ = 25°C | | SN54AHCT74 | | SN74AHCT74 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 5 | | 5 | | 5 | | ns |
| | | CLK | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 5 | | 5 | | 5 | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | 3.5 | | 3.5 | | 3.5 | | |
| $t_h$ | Hold time, data after CLK↑ | | 0 | | 0 | | 0 | | ns |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT74 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 100 | 160 | | 80 | | MHz |
| | | | $C_L$ = 50 pF | 80 | 140 | | 65 | | |
| $t_{PLH}$* | PRE or CLR | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 7.6 | 10.4 | 1 | 12 | ns |
| $t_{PHL}$* | | | | | 7.6 | 10.4 | 1 | 12 | |
| $t_{PLH}$* | CLK | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 5.8 | 7.8 | 1 | 9 | ns |
| $t_{PHL}$* | | | | | 5.8 | 7.8 | 1 | 9 | |
| $t_{PLH}$ | PRE or CLR | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 8.1 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.4 | 1 | 13 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 6.3 | 8.8 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 6.3 | 8.8 | 1 | 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT74 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 100 | 160 | | 80 | | MHz |
| | | | $C_L$ = 50 pF | 80 | 140 | | 65 | | |
| $t_{PLH}$ | PRE or CLR | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 7.6 | 10.4 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.6 | 10.4 | 1 | 12 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 5.8 | 7.8 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.8 | 7.8 | 1 | 9 | |
| $t_{PLH}$ | PRE or CLR | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 8.1 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.4 | 1 | 13 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 6.3 | 8.8 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 6.3 | 8.8 | 1 | 10 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

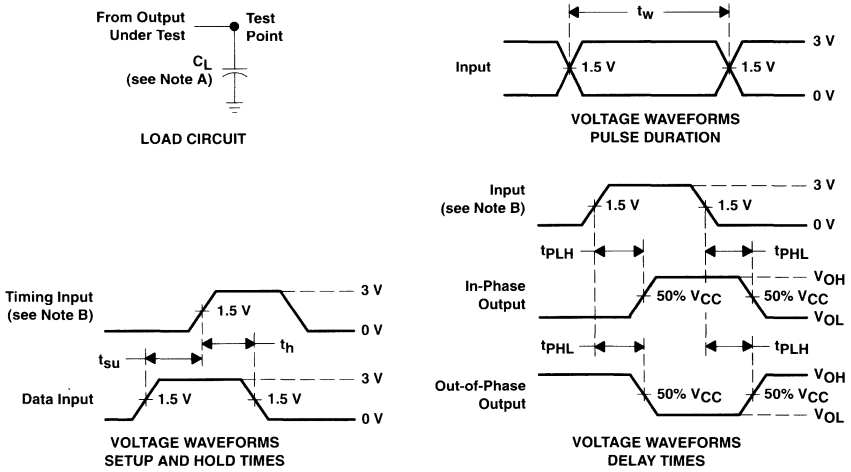
| PARAMETER | | SN74AHCT74 MIN | SN74AHCT74 MAX | UNIT |
|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 32 | pF |

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

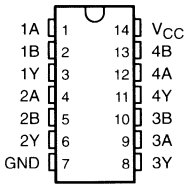
**Figure 1. Load Circuit and Voltage Waveforms**

ADVANCE INFORMATION

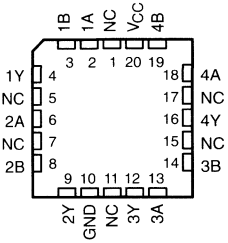
SCLS249B – OCTOBER 1995 – REVISED MAY 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC86 . . . J OR W PACKAGE**
**SN74AHC86 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC86 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC86 are quadruple 2-input exclusive-OR gates. These devices perform the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

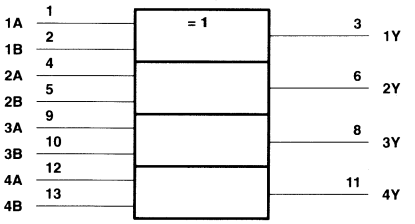
The SN54AHC86 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC86 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

EPIC is a trademark of Texas Instruments Incorporated.

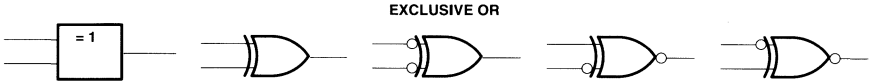
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

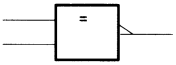
## exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



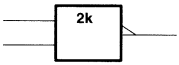

These are five equivalent exclusive-OR symbols valid for an SN74AHCT86 gate in positive logic; negation may be shown at any two ports.

**LOGIC-IDENTITY ELEMENT**



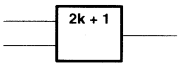

The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

**EVEN-PARITY ELEMENT**




The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

**ODD-PARITY ELEMENT**




The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC86 | | SN74AHC86 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC86 | | SN74AHC86 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | A or B inputs | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | | $V_I = V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC86 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 7 | 11 | 1 | 13 | ns |
| $t_{PHL}$* | | | | | 7 | 11 | 1 | 13 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 9.5 | 14.5 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | | 9.5 | 14.5 | 1 | 16.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC86 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 7 | 11 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 7 | 11 | 1 | 13 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 9.5 | 14.5 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | | 9.5 | 14.5 | 1 | 16.5 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC86 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 4.8 | 6.8 | 1 | 8 | ns |
| $t_{PHL}$* | | | | | 4.8 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 6.3 | 8.8 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 6.3 | 8.8 | 1 | 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC86 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 4.8 | 6.8 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 4.8 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 6.3 | 8.8 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 6.3 | 8.8 | 1 | 10 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

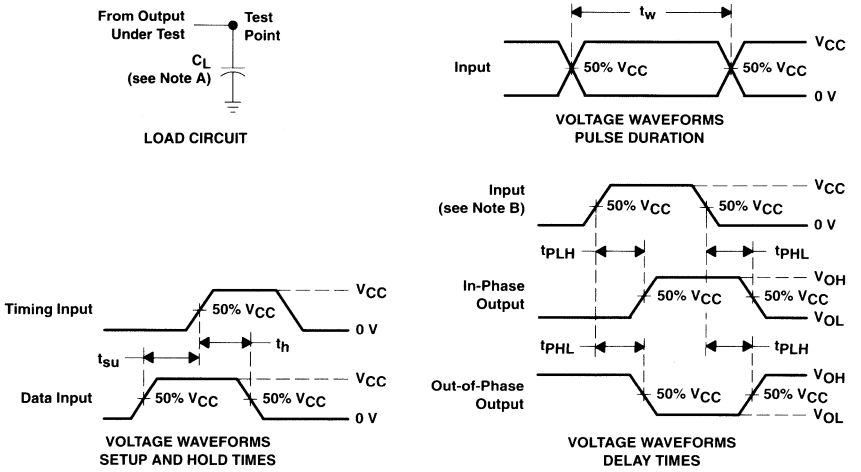
| PARAMETER | | SN74AHC86 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.3 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.3 | –0.8 | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 18 | pF |

## PARAMETER MEASUREMENT INFORMATION



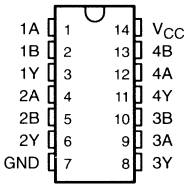

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

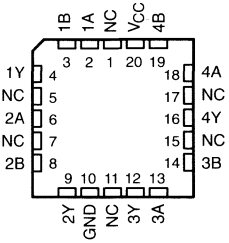
SCLS250E – OCTOBER 1995 – REVISED JUNE 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT86 . . . J OR W PACKAGE**
**SN74AHCT86 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT86 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHCT86 are quadruple 2-input exclusive-OR gates. These devices perform the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

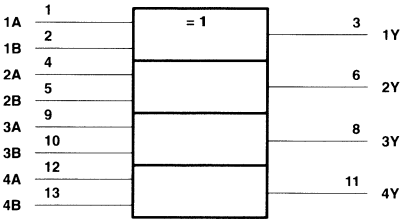
The SN54AHCT86 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT86 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

EPIC is a trademark of Texas Instruments Incorporated.

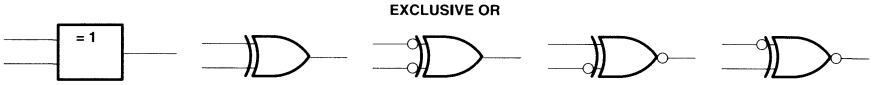
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

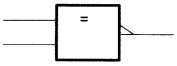
## exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



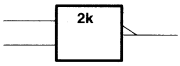

These are five equivalent exclusive-OR symbols valid for an SN74AHCT86 gate in positive logic; negation may be shown at any two ports.

**LOGIC-IDENTITY ELEMENT**



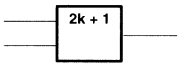

The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

**EVEN-PARITY ELEMENT**




The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

**ODD-PARITY ELEMENT**




The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 127°C/W
DB package . . . . . 158°C/W
DGV package . . . . . 182°C/W
N package . . . . . 78°C/W
PW package . . . . . 170°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT86 | | SN74AHCT86 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT86 | | SN74AHCT86 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT86 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN MAX | |
| | | | | MIN | TYP | MAX | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 8 | ns |
| $t_{PHL}$* | | | | | 5 | 6.9 | 1 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 8.8 | 1 10 | ns |
| $t_{PHL}$ | | | | | 5.5 | 8.8 | 1 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT86 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN MAX | |
| | | | | MIN | TYP | MAX | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 8 | ns |
| $t_{PHL}$ | | | | | 5 | 6.9 | 1 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 8.8 | 1 10 | ns |
| $t_{PHL}$ | | | | | 5.5 | 8.8 | 1 10 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

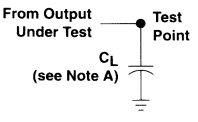
| PARAMETER | | SN74AHCT86 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.4 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

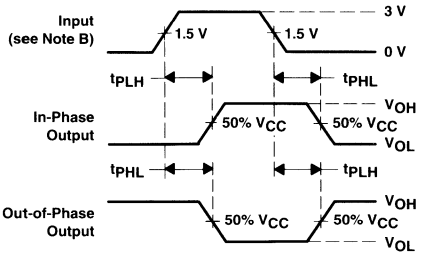
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 18 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT



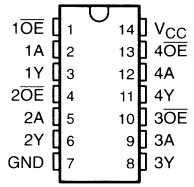

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

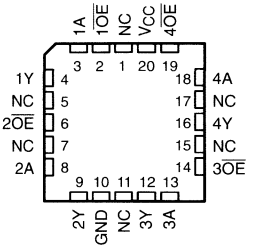
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC125 . . . J OR W PACKAGE**
**SN74AHC125 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC125 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC125 are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, the respective gate passes the data from the A input to its Y output.

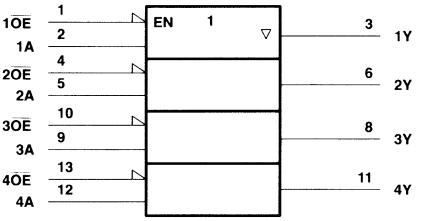
The SN54AHC125 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC125 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| OE | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

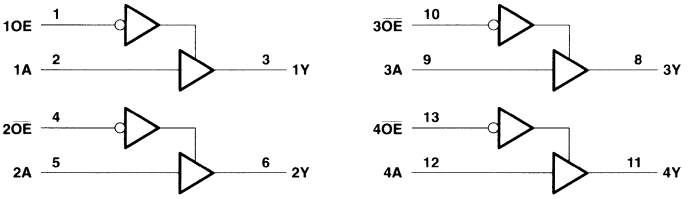
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC125 | | SN74AHC125 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | – 40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC125 | | SN74AHC125 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | A or $\overline{OE}$ inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC125 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5.6 | 8 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.6 | 8 | 1 | 9.5 | |
| $t_{PZH}$* | OE | Y | $C_L$ = 15 pF | | 5.4 | 8 | 1 | 9.5 | ns |
| $t_{PZL}$* | | | | | 5.4 | 8 | 1 | 9.5 | |
| $t_{PHZ}$* | OE | Y | $C_L$ = 15 pF | | 7 | 9.7 | 1 | 11.5 | ns |
| $t_{PLZ}$* | | | | | 7 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 8.1 | 11.5 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.5 | 1 | 13 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 7.9 | 11.5 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 7.9 | 11.5 | 1 | 13 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 9.5 | 13.2 | 1 | 15 | ns |
| $t_{PLZ}$ | | | | | 9.5 | 13.2 | 1 | 15 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC125 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5.6 | 8 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8 | 1 | 9.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 15 pF | | 5.4 | 8 | 1 | 9.5 | ns |
| $t_{PZL}$ | | | | | 5.4 | 8 | 1 | 9.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7 | 9.7 | 1 | 11.5 | ns |
| $t_{PLZ}$ | | | | | 7 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 8.1 | 11.5 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.5 | 1 | 13 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.9 | 11.5 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 7.9 | 11.5 | 1 | 13 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 9.5 | 13.2 | 1 | 15 | ns |
| $t_{PLZ}$ | | | | | 9.5 | 13.2 | 1 | 15 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC125 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 3.6 | 5.1 | 1 | 6 | ns |
| $t_{PZL}$* | | | | | 3.6 | 5.1 | 1 | 6 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$* | | | | | 4.6 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 5.1 | 7.1 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 5.1 | 7.1 | 1 | 8 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC125 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 3.6 | 5.1 | 1 | 6 | ns |
| $t_{PZL}$ | | | | | 3.6 | 5.1 | 1 | 6 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$ | | | | | 4.6 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 5.1 | 7.1 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 5.1 | 7.1 | 1 | 8 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC125 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

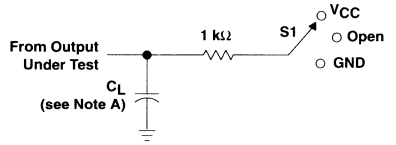
| PARAMETER | | SN74AHC125 MIN | SN74AHC125 MAX | UNIT |
|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.4 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

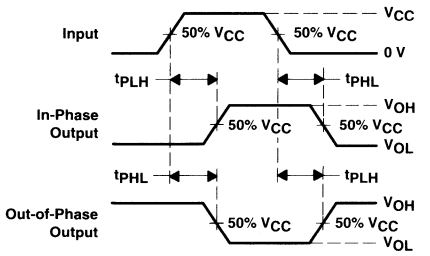
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 14 | pF |

## PARAMETER MEASUREMENT INFORMATION

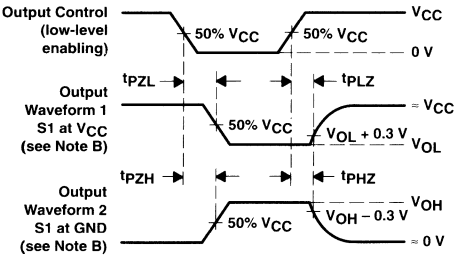



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



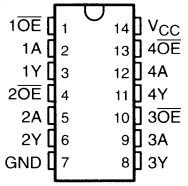

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

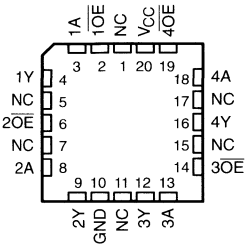
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT125 . . . J OR W PACKAGE**
**SN74AHCT125 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT125 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHCT125 are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, the respective gate passes the data from the A input to its Y output.

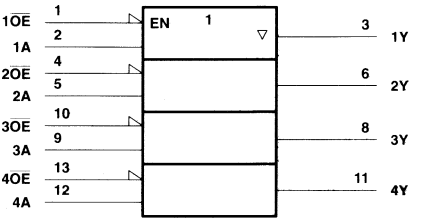
The SN54AHCT125 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT125 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

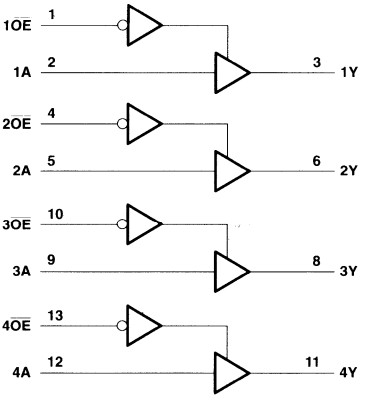
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
DGV package ..... 182°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT125 | | SN74AHCT125 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT125 | | SN74AHCT125 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | A or $\overline{OE}$ inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$‡ | | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |
| $C_o$ | | $V_O$ = $V_{CC}$ or GND | 5 V | | 15 | | | | | | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT125 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$* | OE | Y | $C_L$ = 15 pF | | 3.6 | 5.1 | 1 | 6 | ns |
| $t_{PZL}$* | | | | | 3.6 | 5.1 | 1 | 6 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$* | | | | | 4.6 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 5.1 | 7.1 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 5.1 | 7.1 | 1 | 8 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT125 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 3.6 | 5.1 | 1 | 6 | ns |
| $t_{PZL}$ | | | | | 3.6 | 5.1 | 1 | 6 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$ | | | | | 4.6 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 5.1 | 7.1 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 5.1 | 7.1 | 1 | 8 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74AHCT125 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | | MIN | MAX | | | |
| $t_{sk(o)}$ | A | Y | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

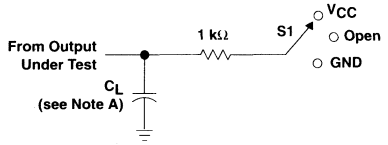
| PARAMETER | | SN74AHCT125 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.4 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

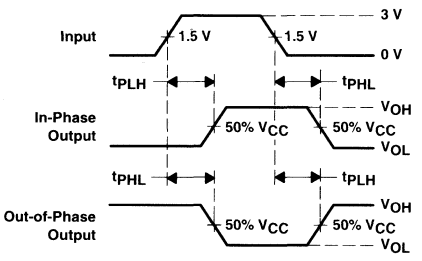
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 14 | pF |

## PARAMETER MEASUREMENT INFORMATION

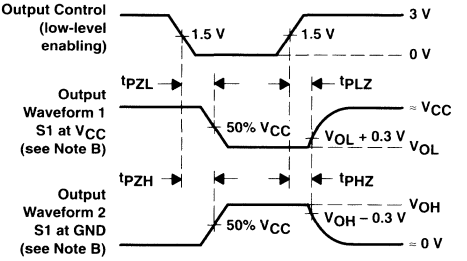



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



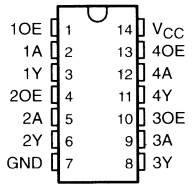

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

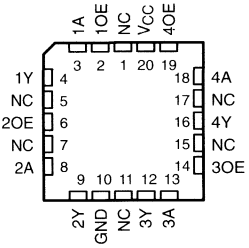
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC126 . . . J OR W PACKAGE**
**SN74AHC126 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC126 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC126 are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output.

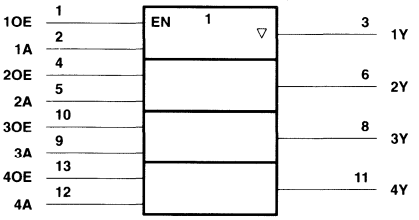
The SN54AHC126 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC126 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| OE | A | Y |
| H | H | H |
| H | L | L |
| L | X | Z |

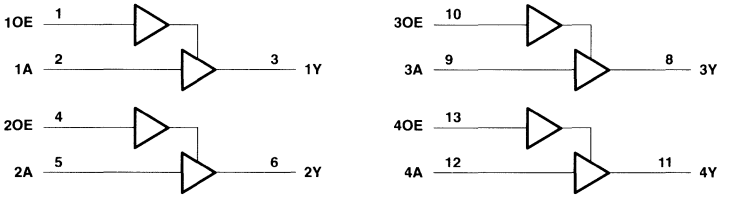
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC126 | | SN74AHC126 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | – 40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC126 | | SN74AHC126 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | A or OE inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC126 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5.6 | 8 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.6 | 8 | 1 | 9.5 | |
| $t_{PZH}$* | OE | Y | $C_L$ = 15 pF | | 5.4 | 8 | 1 | 9.5 | ns |
| $t_{PZL}$* | | | | | 5.4 | 8 | 1 | 9.5 | |
| $t_{PHZ}$* | OE | Y | $C_L$ = 15 pF | | 7 | 9.7 | 1 | 11.5 | ns |
| $t_{PLZ}$* | | | | | 7 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 8.1 | 11.5 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.5 | 1 | 13 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 7.9 | 11.5 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 7.9 | 11.5 | 1 | 13 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 9.5 | 13.2 | 1 | 15 | ns |
| $t_{PLZ}$ | | | | | 9.5 | 13.2 | 1 | 15 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC126 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5.6 | 8 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8 | 1 | 9.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 15 pF | | 5.4 | 8 | 1 | 9.5 | ns |
| $t_{PZL}$ | | | | | 5.4 | 8 | 1 | 9.5 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 15 pF | | 7 | 9.7 | 1 | 11.5 | ns |
| $t_{PLZ}$ | | | | | 7 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 8.1 | 11.5 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.5 | 1 | 13 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 7.9 | 11.5 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 7.9 | 11.5 | 1 | 13 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 9.5 | 13.2 | 1 | 15 | ns |
| $t_{PLZ}$ | | | | | 9.5 | 13.2 | 1 | 15 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC126 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$* | OE | Y | $C_L$ = 15 pF | | 3.6 | 5.1 | 1 | 6 | ns |
| $t_{PZL}$* | | | | | 3.6 | 5.1 | 1 | 6 | |
| $t_{PHZ}$* | OE | Y | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$* | | | | | 4.6 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 5.1 | 7.1 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 5.1 | 7.1 | 1 | 8 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC126 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 15 pF | | 3.6 | 5.1 | 1 | 6 | ns |
| $t_{PZL}$ | | | | | 3.6 | 5.1 | 1 | 6 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$ | | | | | 4.6 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 5.1 | 7.1 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 5.1 | 7.1 | 1 | 8 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC126 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

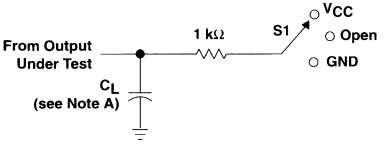
| PARAMETER | | SN74AHC126 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.4 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

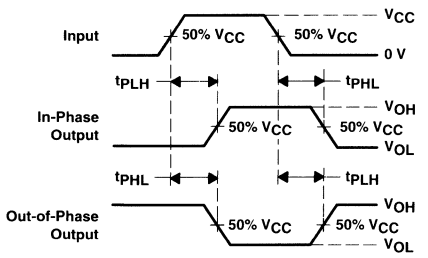
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 14 | pF |

## PARAMETER MEASUREMENT INFORMATION

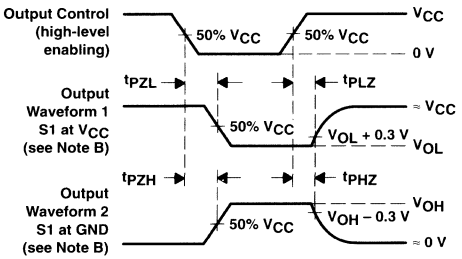



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

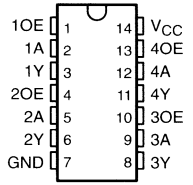
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

## description

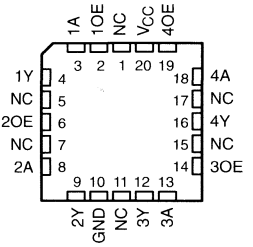
The 'AHCT126 are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output.

The SN54AHCT126 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT126 is characterized for operation from –40°C to 85°C.

**SN54AHCT126 . . . J OR W PACKAGE**
**SN74AHCT126 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT126 . . . FK PACKAGE**
**(TOP VIEW)**



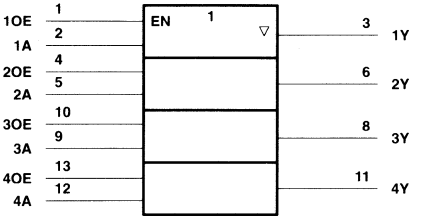

NC – No internal connection

**FUNCTION TABLE**
**(each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| OE | A | Y |
| H | H | H |
| H | L | L |
| L | X | Z |

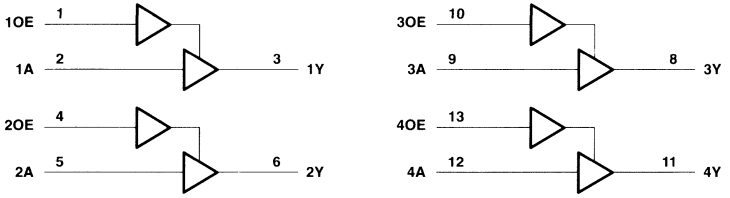
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
DGV package ..... 182°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT126 | | SN74AHCT126 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT126 | | SN74AHCT126 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | A or OE inputs | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{OZ}$ | | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | | $V_I = V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |
| $C_o$ | | $V_O = V_{CC}$ or GND | 5 V | | 15 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT126 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$* | OE | Y | $C_L$ = 15 pF | | 3.6 | 5.1 | 1 | 6 | ns |
| $t_{PZL}$* | | | | | 3.6 | 5.1 | 1 | 6 | |
| $t_{PHZ}$* | OE | Y | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$* | | | | | 4.6 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 5.1 | 7.1 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 5.1 | 7.1 | 1 | 8 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT126 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 15 pF | | 3.6 | 5.1 | 1 | 6 | ns |
| $t_{PZL}$ | | | | | 3.6 | 5.1 | 1 | 6 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$ | | | | | 4.6 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 5.1 | 7.1 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 5.1 | 7.1 | 1 | 8 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74AHCT126 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | | MIN | MAX | | | |
| $t_{sk(o)}$ | A | Y | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

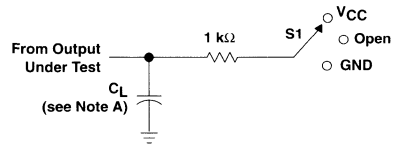
| PARAMETER | | SN74AHCT126 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.4 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

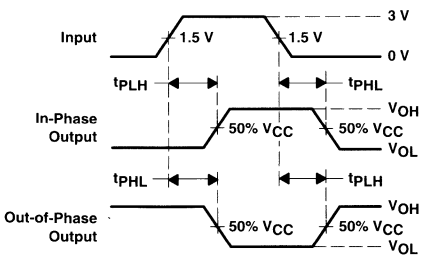
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 14 | pF |

## PARAMETER MEASUREMENT INFORMATION

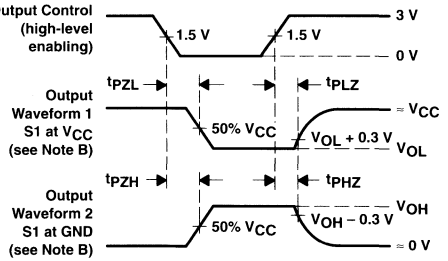



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



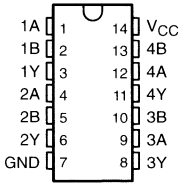

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

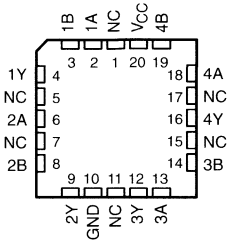
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Operation From Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Same Pinouts as 'AHC00**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC132 . . . J OR W PACKAGE**
**SN74AHC132 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC132 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The 'AHC132 perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54AHC132 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC132 is characterized for operation from –40°C to 85°C.

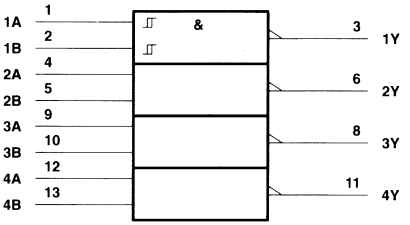
**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

PRODUCT PREVIEW

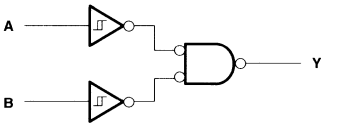
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC132 | | SN74AHC132 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC132 | | SN74AHC132 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{T+}$ Positive-going input threshold voltage | | 3 V | | | 2.2 | | 2.2 | | 2.2 | V |
| | | 4.5 V | | | 3.15 | | 3.15 | | 3.15 | |
| | | 5.5 V | | | 3.85 | | 3.85 | | 3.85 | |
| $V_{T-}$ Negative-going input threshold voltage | | 3 V | 0.9 | | | 0.9 | | 0.9 | | V |
| | | 4.5 V | 1.35 | | | 1.35 | | 1.35 | | |
| | | 5.5 V | 1.65 | | | 1.65 | | 1.65 | | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | 3 V | 0.3 | | 1.2 | 0.3 | 1.2 | 0.3 | 1.2 | V |
| | | 4.5 V | 0.4 | | 1.4 | 0.4 | 1.4 | 0.4 | 1.4 | |
| | | 5.5 V | 0.5 | | 1.6 | 0.5 | 1.6 | 0.5 | 1.6 | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC132 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 5.5 | 7.9 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.5 | 7.9 | 1 | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8 | 11.4 | 1 | 13 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC132 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5.5 | 7.9 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8 | 11.4 | 1 | 13 | |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC132 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 3.7 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.7 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.2 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.2 | 7.5 | 1 | 8.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC132 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 3.7 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.7 | 5.5 | 1 | 6.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.2 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.2 | 7.5 | 1 | 8.5 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

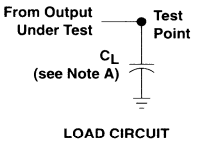
| PARAMETER | | SN74AHC132 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.3 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.3 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.6 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

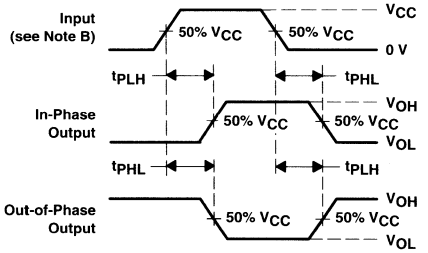
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

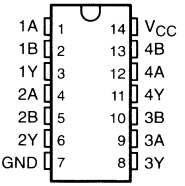
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

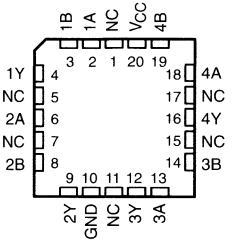
PRODUCT PREVIEW

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Operation From Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Same Pinouts as 'AHCT00**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT132 . . . J OR W PACKAGE**
**SN74AHCT132 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT132 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The 'AHCT132 perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54AHCT132 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT132 is characterized for operation from –40°C to 85°C.

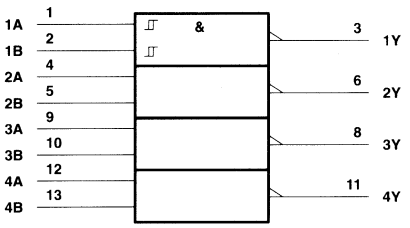
**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

PRODUCT PREVIEW

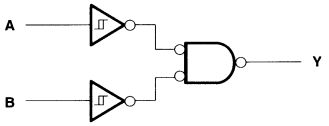
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 127°C/W
DB package ..... 158°C/W
N package ..... 78°C/W
PW package ..... 170°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT132 | | SN74AHCT132 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT132 | | SN74AHCT132 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{T+}$ Positive-going input threshold voltage | | 4.5 V | | | 1.9 | | 1.9 | | 1.9 | V |
| | | 5.5 V | | | 2.1 | | 2.1 | | 2.1 | |
| $V_{T-}$ Negative-going input threshold voltage | | 4.5 V | 0.5 | | | 0.5 | | 0.5 | | V |
| | | 5.5 V | 0.6 | | | 0.6 | | 0.6 | | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | 4.5 V | 0.4 | | 1.4 | 0.4 | 1.4 | 0.4 | 1.4 | V |
| | | 5.5 V | 0.4 | | 1.5 | 0.4 | 1.5 | 0.4 | 1.5 | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT132 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 | 8 | ns |
| $t_{PHL}$* | | | | | 5 | 6.9 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT132 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 6.9 | 1 | 8 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

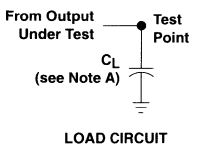
| PARAMETER | | SN74AHCT132 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.5 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

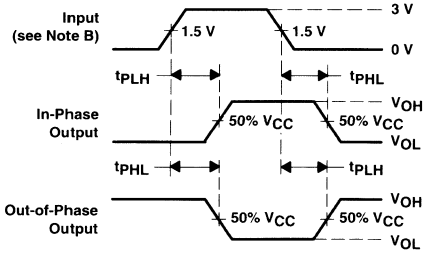
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

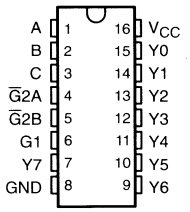
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

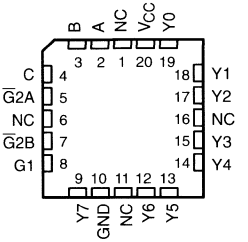
SCLS258D – DECEMBER 1995 – REVISED MAY 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC138 . . . J OR W PACKAGE**
**SN74AHC138 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC138 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC138 decoders/demultiplexers are designed for high-performance memory-decoding or data-routing applications requiring very short propagation-delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54AHC138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC138 is characterized for operation from –40°C to 85°C.

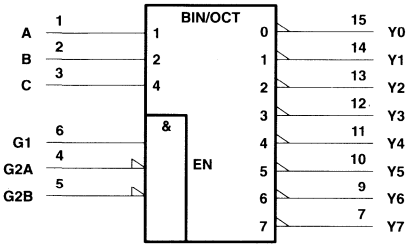
PRODUCT PREVIEW

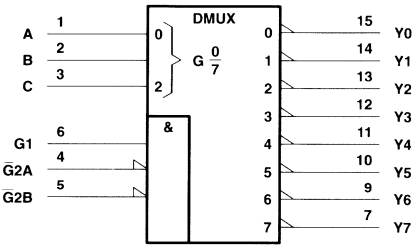
EPIC is a trademark of Texas Instruments Incorporated.

**FUNCTION TABLE**

| ENABLE INPUTS | | | SELECT INPUTS | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | G2A | G2B | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

## logic symbols (alternatives)†

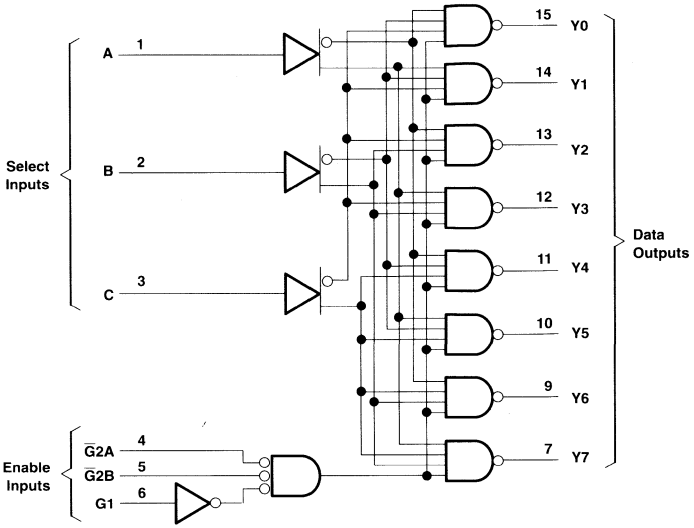



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
N package . . . . . 78°C/W
PW package . . . . . 149°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

## recommended operating conditions (see Note 3)

| | | | SN54AHC138 | | SN74AHC138 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC138 | | SN74AHC138 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC138 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A, B, C | Any Y | $C_L$ = 15 pF | | 8.2 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$* | | | | | 8.2 | 11.4 | 1 | 13 | |
| $t_{PLH}$* | G1 | Any Y | $C_L$ = 15 pF | | 8.1 | 12.8 | 1 | 15 | ns |
| $t_{PHL}$* | | | | | 8.1 | 12.8 | 1 | 15 | |
| $t_{PLH}$* | $\overline{G}$2A, $\overline{G}$2B | Any Y | $C_L$ = 15 pF | | 8.2 | 11.4 | 1 | 13.5 | ns |
| $t_{PHL}$* | | | | | 8.2 | 11.4 | 1 | 13.5 | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 50 pF | | 10 | 15.8 | 1 | 18 | ns |
| $t_{PHL}$ | | | | | 10 | 15.8 | 1 | 18 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 50 pF | | 10.6 | 16.3 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.6 | 16.3 | 1 | 18.5 | |
| $t_{PLH}$ | $\overline{G}$2A, $\overline{G}$2B | Any Y | $C_L$ = 50 pF | | 10.7 | 14.9 | 1 | 17 | ns |
| $t_{PHL}$ | | | | | 10.7 | 14.9 | 1 | 17 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC138 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 15 pF | | 8.2 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.2 | 11.4 | 1 | 13 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 15 pF | | 8.1 | 12.8 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.1 | 12.8 | 1 | 15 | |
| $t_{PLH}$ | $\overline{G}$2A, $\overline{G}$2B | Any Y | $C_L$ = 15 pF | | 8.2 | 11.4 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 8.2 | 11.4 | 1 | 13.5 | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 50 pF | | 10 | 15.8 | 1 | 18 | ns |
| $t_{PHL}$ | | | | | 10 | 15.8 | 1 | 18 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 50 pF | | 10.6 | 16.3 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.6 | 16.3 | 1 | 18.5 | |
| $t_{PLH}$ | $\overline{G}$2A, $\overline{G}$2B | Any Y | $C_L$ = 50 pF | | 10.7 | 14.9 | 1 | 17 | ns |
| $t_{PHL}$ | | | | | 10.7 | 14.9 | 1 | 17 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC138 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A, B, C | Any Y | $C_L$ = 15 pF | | 5.7 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.7 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | G1 | Any Y | $C_L$ = 15 pF | | 5.6 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.6 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | G2A, G2B | Any Y | $C_L$ = 15 pF | | 5.8 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.8 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 50 pF | | 7.2 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 7.2 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 50 pF | | 7.1 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | G2A, G2B | Any Y | $C_L$ = 50 pF | | 7.3 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 7.3 | 10.1 | 1 | 11.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

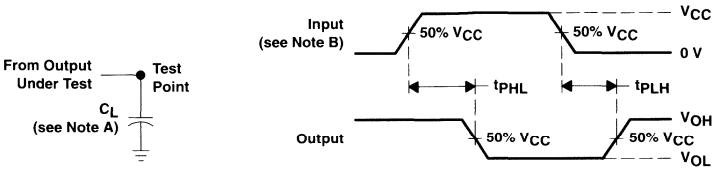
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC138 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 15 pF | | 5.7 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.7 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 15 pF | | 5.6 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{G}$2A, $\overline{G}$2B | Any Y | $C_L$ = 15 pF | | 5.8 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.8 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 50 pF | | 7.2 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 7.2 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 50 pF | | 7.1 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | G2A, $\overline{G}$2B | Any Y | $C_L$ = 50 pF | | 7.3 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 7.3 | 10.1 | 1 | 11.5 | |

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 34 | pF |

PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

## APPLICATION INFORMATION

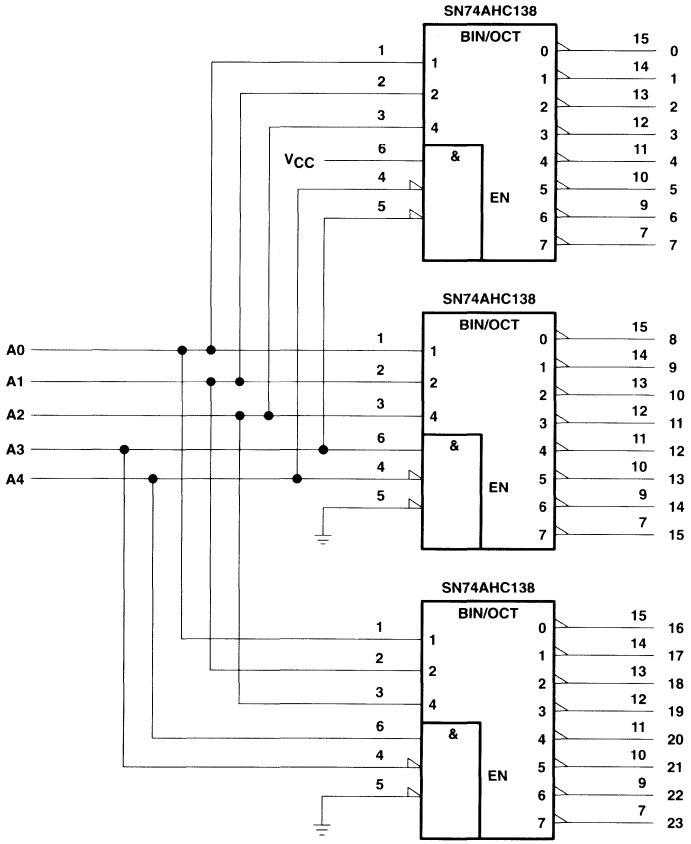



Figure 2. 24-Bit Decoding Scheme

## APPLICATION INFORMATION

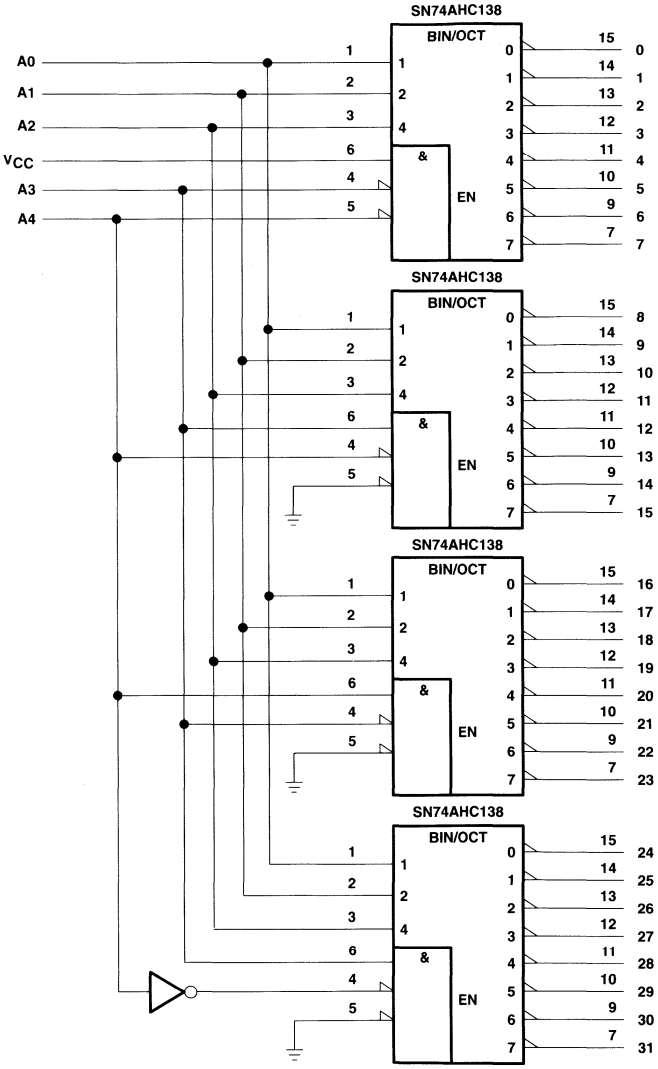
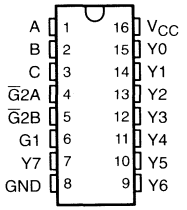


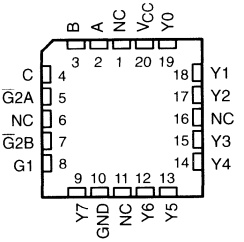

**Figure 3. 32-Bit Decoding Scheme**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT138 . . . J OR W PACKAGE**
**SN74AHCT138 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT138 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHCT138 3-line to 8-line decoders/demultiplexers are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54AHCT138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT138 is characterized for operation from –40°C to 85°C.

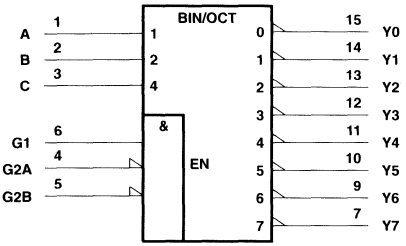
PRODUCT PREVIEW

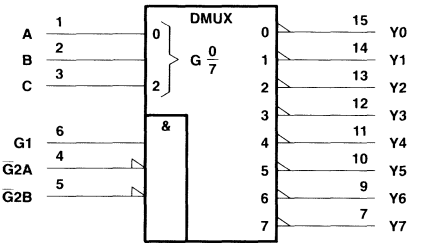
EPIC is a trademark of Texas Instruments Incorporated.

**FUNCTION TABLE**

| ENABLE INPUTS | | | SELECT INPUTS | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | G2A | G2B | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

## logic symbols (alternatives)†

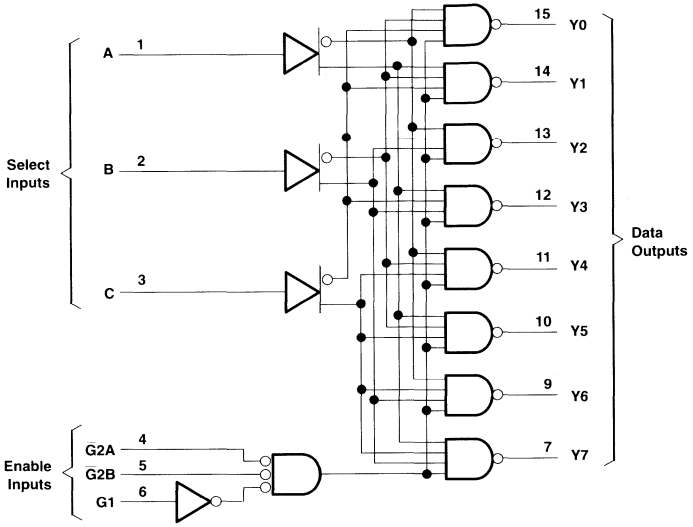



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

## recommended operating conditions (see Note 3)

| | | SN54AHCT138 | | SN74AHCT138 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT138 | | SN74AHCT138 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT138 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A, B, C | Any Y | $C_L$ = 15 pF | | 7.6 | 10.4 | 1 | 12 | ns |
| $t_{PHL}$* | | | | | 7.6 | 10.4 | 1 | 12 | |
| $t_{PLH}$* | G1 | Any Y | $C_L$ = 15 pF | | 6.6 | 9.1 | 1 | 10.5 | ns |
| $t_{PHL}$* | | | | | 6.6 | 9.1 | 1 | 10.5 | |
| $t_{PLH}$* | $\overline{G}$2A, $\overline{G}$2B | Any Y | $C_L$ = 15 pF | | 7 | 9.6 | 1 | 11 | ns |
| $t_{PHL}$* | | | | | 7 | 9.6 | 1 | 11 | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 50 pF | | 8.1 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.4 | 1 | 13 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 50 pF | | 7.1 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | $\overline{G}$2A, $\overline{G}$2B | Any Y | $C_L$ = 50 pF | | 7.5 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.5 | 10.6 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

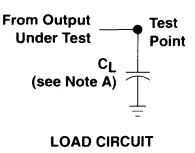
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT138 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 15 pF | | 7.6 | 10.4 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.6 | 10.4 | 1 | 12 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 15 pF | | 6.6 | 9.1 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.6 | 9.1 | 1 | 10.5 | |
| $t_{PLH}$ | $\overline{G}$2A, $\overline{G}$2B | Any Y | $C_L$ = 15 pF | | 7 | 9.6 | 1 | 11 | ns |
| $t_{PHL}$ | | | | | 7 | 9.6 | 1 | 11 | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 50 pF | | 8.1 | 11.4 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.4 | 1 | 13 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 50 pF | | 7.1 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | $\overline{G}$2A, $\overline{G}$2B | Any Y | $C_L$ = 50 pF | | 7.5 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.5 | 10.6 | 1 | 12 | |

**operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C**

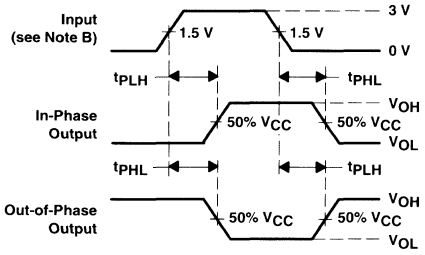
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 49 | pF |

PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

## APPLICATION INFORMATION

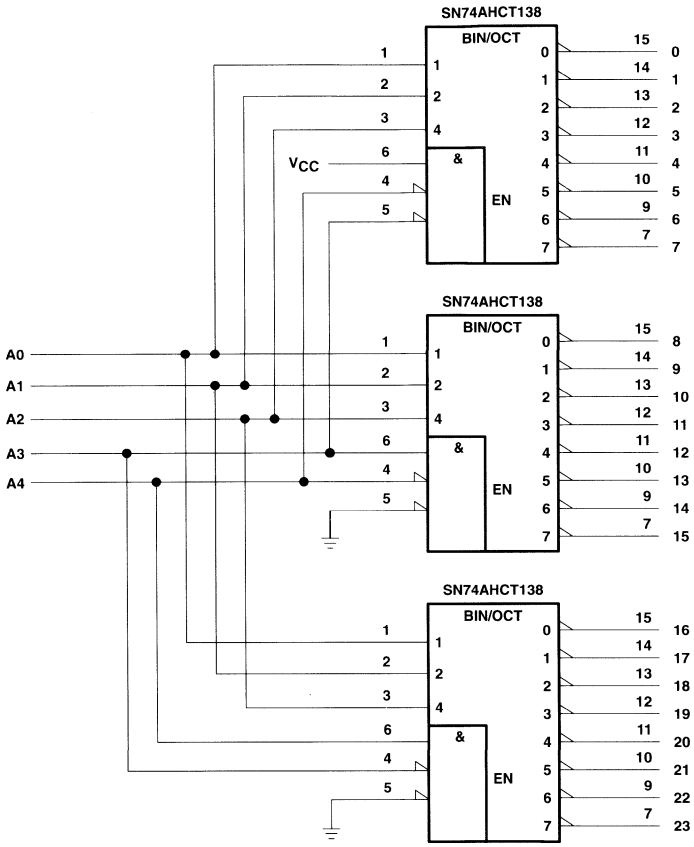



**Figure 2. 24-Bit Decoding Scheme**

## APPLICATION INFORMATION

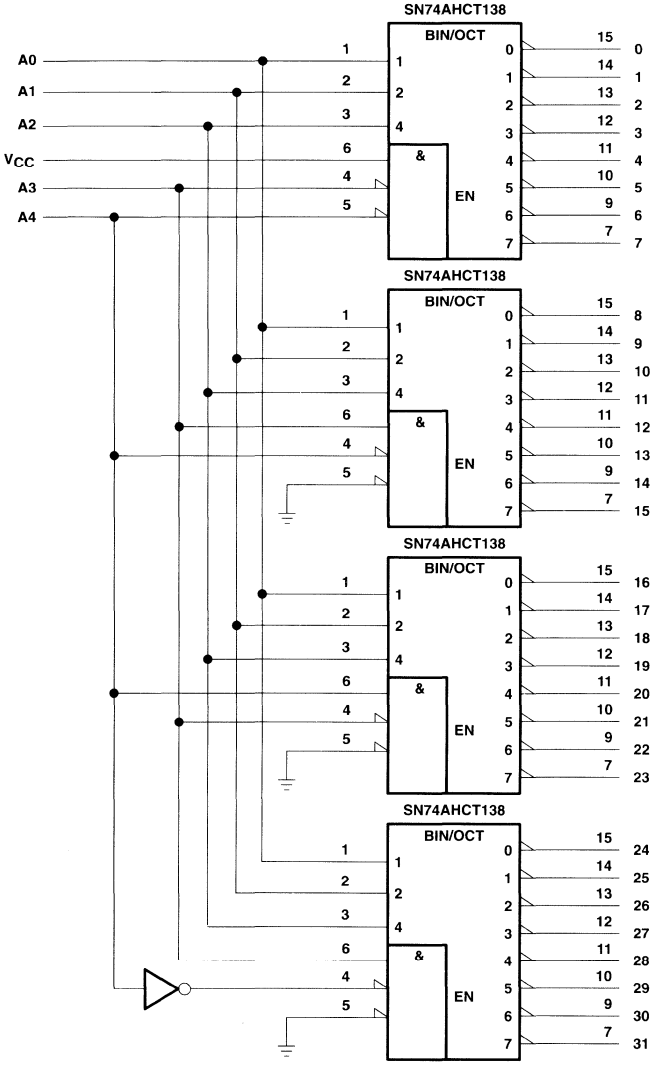
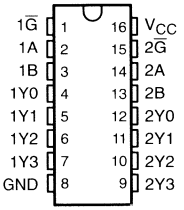



Figure 3. 32-Bit Decoding Scheme

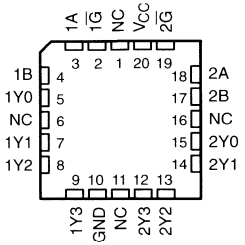
SCLS259D – DECEMBER 1995 – REVISED MAY 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC139 . . . J OR W PACKAGE**
**SN74AHC139 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC139 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC139 are dual 2-line to 4-line decoders/demultiplexers designed for 2-V to 5.5-V $V_{CC}$ operation. These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The active-low enable ($\overline{G}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN54AHC139 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC139 is characterized for operation from –40°C to 85°C.

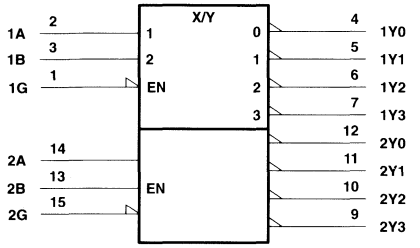
PRODUCT PREVIEW

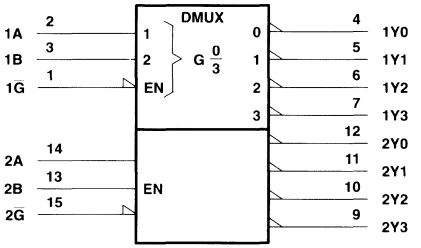
EPIC is a trademark of Texas Instruments Incorporated.

**FUNCTION TABLE**

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| G | SELECT | | | | | |
| | B | A | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

## logic symbols (alternatives)†

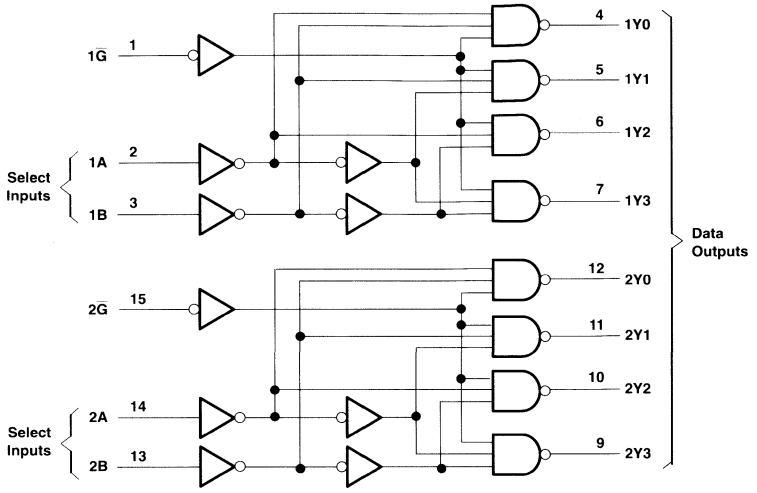



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

### recommended operating conditions (see Note 3)

| | | | SN54AHC139 | | SN74AHC139 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC139 | | SN74AHC139 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC139 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 7.2 | 11 | 1 | 13 | ns |
| $t_{PHL}$* | | | | | 7.2 | 11 | 1 | 13 | |
| $t_{PLH}$* | $\overline{G}$ | Y | $C_L$ = 15 pF | | 6.4 | 9.2 | 1 | 11 | ns |
| $t_{PHL}$* | | | | | 6.4 | 9.2 | 1 | 11 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 9.7 | 14.5 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | | 9.7 | 14.5 | 1 | 16.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 8.9 | 12.7 | 1 | 14.5 | ns |
| $t_{PHL}$ | | | | | 8.9 | 12.7 | 1 | 14.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC139 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 7.2 | 11 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 7.2 | 11 | 1 | 13 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 15 pF | | 6.4 | 9.2 | 1 | 11 | ns |
| $t_{PHL}$ | | | | | 6.4 | 9.2 | 1 | 11 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 9.7 | 14.5 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | | 9.7 | 14.5 | 1 | 16.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 8.9 | 12.7 | 1 | 14.5 | ns |
| $t_{PHL}$ | | | | | 8.9 | 12.7 | 1 | 14.5 | |

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC139 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 5 | 7.2 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5 | 7.2 | 1 | 8.5 | |
| $t_{PLH}$* | G | Y | $C_L$ = 15 pF | | 4.4 | 6.3 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 4.4 | 6.3 | 1 | 7.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 6.5 | 9.2 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.5 | 9.2 | 1 | 10.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 5.9 | 8.3 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.9 | 8.3 | 1 | 9.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

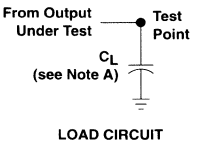
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC139 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5 | 7.2 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5 | 7.2 | 1 | 8.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 15 pF | | 4.4 | 6.3 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 4.4 | 6.3 | 1 | 7.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 6.5 | 9.2 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.5 | 9.2 | 1 | 10.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 5.9 | 8.3 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.9 | 8.3 | 1 | 9.5 | |

PRODUCT PREVIEW

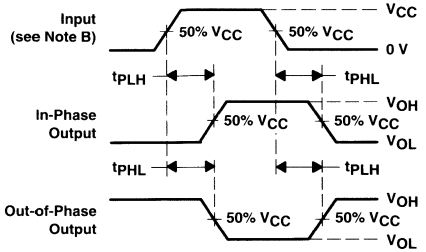
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 26 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

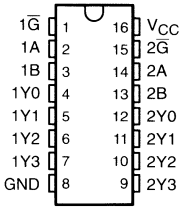
**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

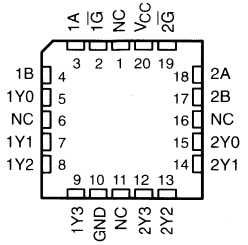
SCLS267E – DECEMBER 1995 – REVISED MAY 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT139 . . . J OR W PACKAGE**
**SN74AHCT139 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT139 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHCT139 are dual 2-line to 4-line decoders/demultiplexers designed for 4.5-V to 5.5-V $V_{CC}$ operation. These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The active-low enable ($\overline{G}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN54AHCT139 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT139 is characterized for operation from –40°C to 85°C.

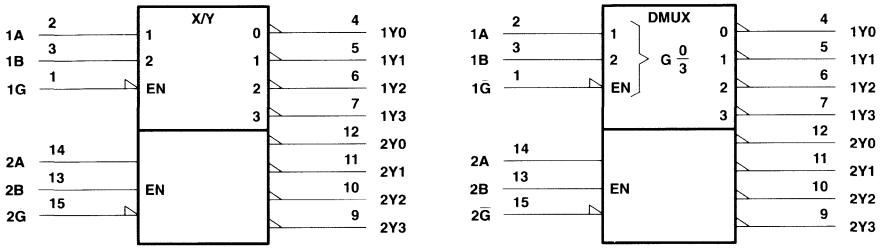
PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

**FUNCTION TABLE**

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| $\overline{G}$ | SELECT | | | | | |
| | B | A | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

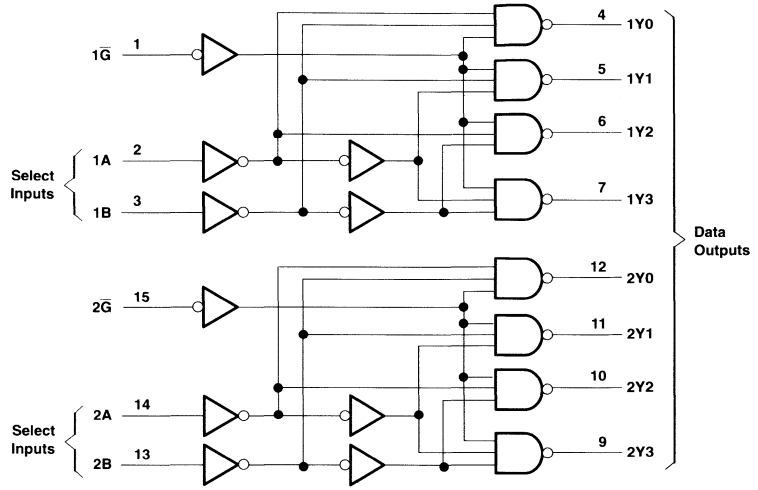
## logic symbols (alternatives)†




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I < 0$) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

## recommended operating conditions (see Note 3)

| | | SN54AHCT139 | | SN74AHCT139 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT139 | | SN74AHCT139 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 4.5 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT139 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | | | 1 | | ns |
| $t_{PHL}$* | | | | | | | 1 | | |
| $t_{PLH}$* | $\overline{G}$ | Y | $C_L$ = 15 pF | | | | 1 | | ns |
| $t_{PHL}$* | | | | | | | 1 | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | | | 1 | | ns |
| $t_{PHL}$ | | | | | | | 1 | | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | | | 1 | | ns |
| $t_{PHL}$ | | | | | | | 1 | | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

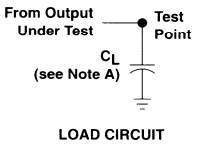
**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT139 $T_A$ = 25°C MIN | SN74AHCT139 $T_A$ = 25°C TYP | SN74AHCT139 $T_A$ = 25°C MAX | SN74AHCT139 MIN | SN74AHCT139 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | | | 1 | | ns |
| $t_{PHL}$ | | | | | | | 1 | | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 15 pF | | | | 1 | | ns |
| $t_{PHL}$ | | | | | | | 1 | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | | | 1 | | ns |
| $t_{PHL}$ | | | | | | | 1 | | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | | | 1 | | ns |
| $t_{PHL}$ | | | | | | | 1 | | |

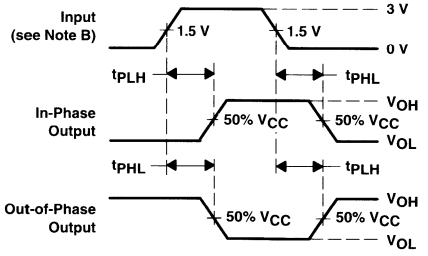
**operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C**

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 26 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

SCLS345A – MAY 1996 – REVISED MAY 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

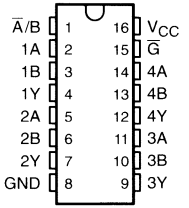
## description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 2-V to 5.5-V $V_{CC}$ operation.

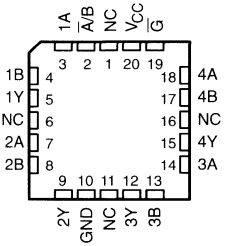
The 'AHC157 feature a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.

The SN54AHC157 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC157 is characterized for operation from –40°C to 85°C.

**SN54AHC157 . . . J OR W PACKAGE**
**SN74AHC157 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC157 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

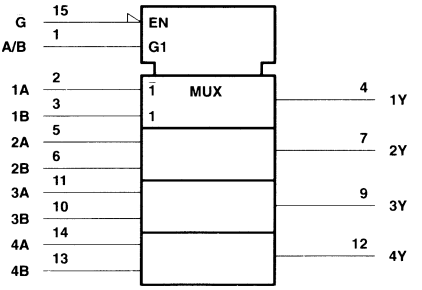
**FUNCTION TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{G}$ | A/B | A | B | Y |
| H | X | X | X | L |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

PRODUCT PREVIEW

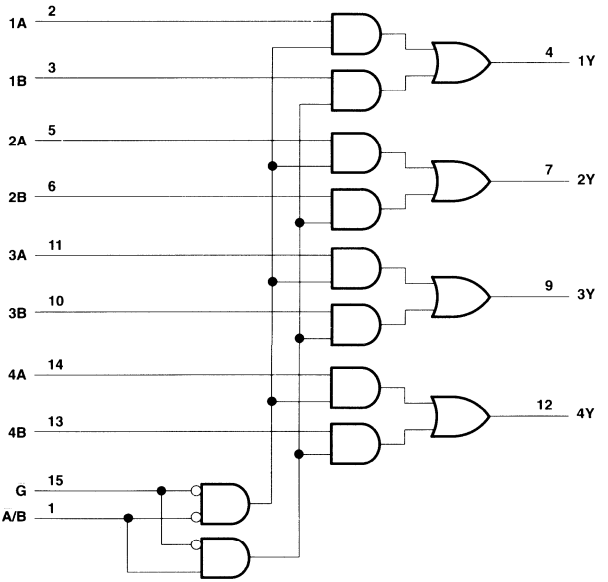
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | | SN54AHC157 | | SN74AHC157 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC157 | | SN74AHC157 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | A or B inputs | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | | $V_I = V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC157 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 6.2 | 9.7 | 1 | 11.5 | ns |
| $t_{PHL}$* | | | | | 6.2 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$* | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 8.4 | 13.2 | 1 | 15.5 | ns |
| $t_{PHL}$* | | | | | 8.4 | 13.2 | 1 | 15.5 | |
| $t_{PLH}$* | $\overline{G}$ | Y | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PHL}$* | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.7 | 13.2 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.2 | 1 | 15 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 10.9 | 16.7 | 1 | 19 | ns |
| $t_{PHL}$ | | | | | 10.9 | 16.7 | 1 | 19 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC157 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 6.2 | 9.7 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.2 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 8.4 | 13.2 | 1 | 15.5 | ns |
| $t_{PHL}$ | | | | | 8.4 | 13.2 | 1 | 15.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.7 | 13.2 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.2 | 1 | 15 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 10.9 | 16.7 | 1 | 19 | ns |
| $t_{PLH}$ | | | | | 10.9 | 16.7 | 1 | 19 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC157 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$* | A/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | $\overline{G}$ | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PLH}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC157 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PLH}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |

**noise characteristics $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)**

| PARAMETER | | SN74AHC157 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

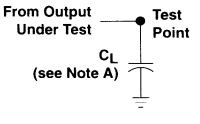
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

PRODUCT PREVIEW

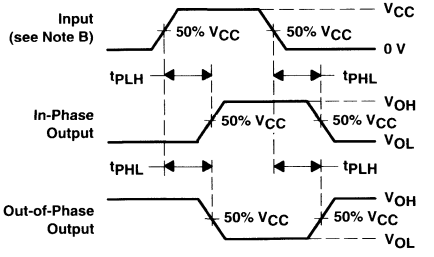
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 20 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

SCLS347D – MAY 1996 – REVISED MAY 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

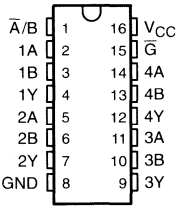
## description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V $V_{CC}$ operation.

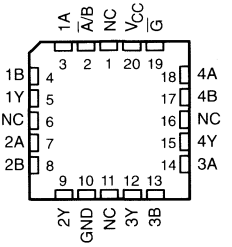
The 'AHCT157 feature a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.

The SN54AHCT157 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT157 is characterized for operation from –40°C to 85°C.

**SN54AHCT157 . . . J OR W PACKAGE**
**SN74AHCT157 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT157 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

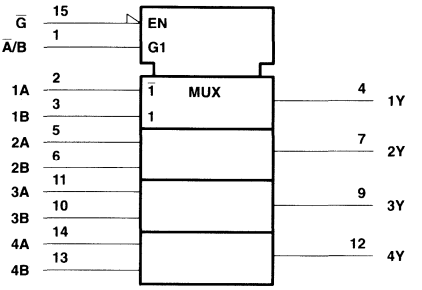
**FUNCTION TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{G}$ | A/B | A | B | Y |
| H | X | X | X | L |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

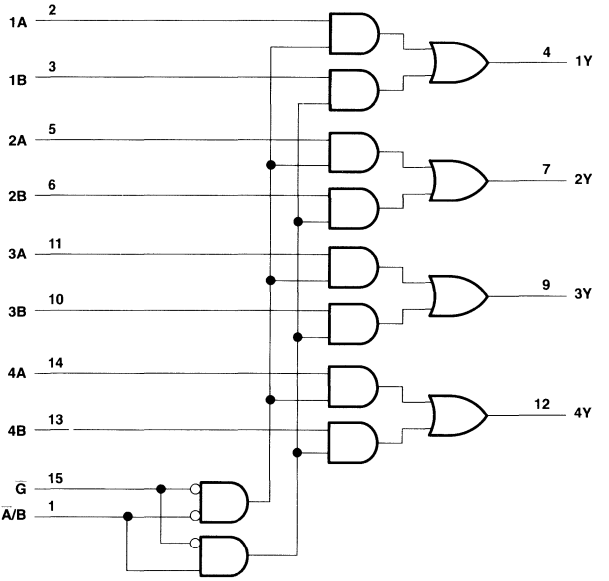
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.



## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
N package . . . . . 78°C/W
PW package . . . . . 149°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT157 | | SN74AHCT157 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall time | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT157 | | SN74AHCT157 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | µA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4.5 | | | | | | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT157 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$* | A/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | G | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | A/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PLH}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | G | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT157 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | G | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PLH}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |

### noise characteristics $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

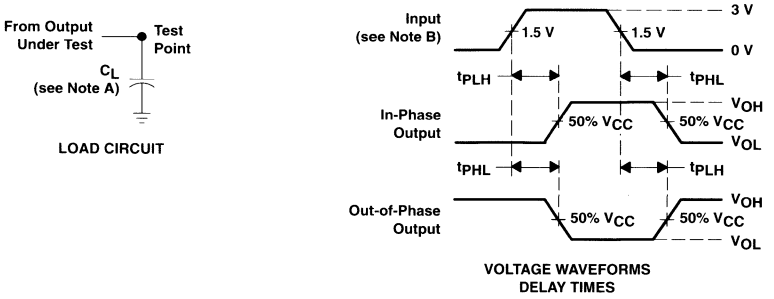
| PARAMETER | | SN74AHCT157 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 26 | pF |

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

SCLS346A – MAY 1996 – REVISED APRIL 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

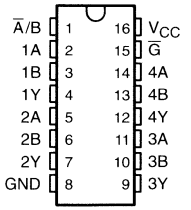
## description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 2-V to 5.5-V $V_{CC}$ operation.

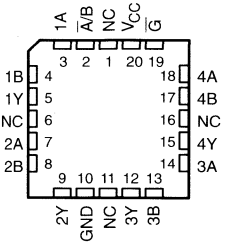
The 'AHC158 feature a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. These devices provide inverted data.

The SN54AHC158 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC158 is characterized for operation from –40°C to 85°C.

**SN54AHC158 . . . J OR W PACKAGE**
**SN74AHC158 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC158 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

**FUNCTION TABLE**

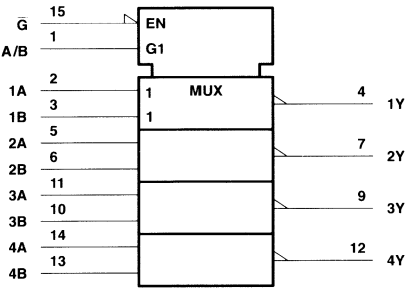
| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{G}$ | A/B | A | B | Y |
| H | X | X | X | H |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

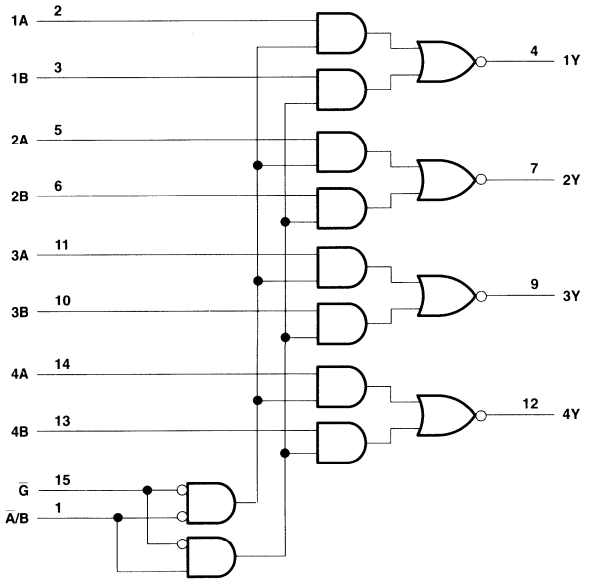
PRODUCT PREVIEW

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
N package . . . . . 78°C/W
PW package . . . . . 149°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC158 | | SN74AHC158 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC158 | | SN74AHC158 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | A or B inputs | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | | $V_I = V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC158 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 6.2 | 9.7 | 1 | 11.5 | ns |
| $t_{PHL}$* | | | | | 6.2 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$* | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 8.4 | 13.2 | 1 | 15.5 | ns |
| $t_{PHL}$* | | | | | 8.4 | 13.2 | 1 | 15.5 | |
| $t_{PLH}$* | $\overline{G}$ | Y | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PHL}$* | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.7 | 13.2 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.2 | 1 | 15 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 10.9 | 16.7 | 1 | 19 | ns |
| $t_{PHL}$ | | | | | 10.9 | 16.7 | 1 | 19 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC158 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 6.2 | 9.7 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.2 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 8.4 | 13.2 | 1 | 15.5 | ns |
| $t_{PHL}$ | | | | | 8.4 | 13.2 | 1 | 15.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.7 | 13.2 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.2 | 1 | 15 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 10.9 | 16.7 | 1 | 19 | ns |
| $t_{PLH}$ | | | | | 10.9 | 16.7 | 1 | 19 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC158 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$* | A/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | G | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | A/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PLH}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | G | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC158 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | G | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PLH}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |

**noise characteristics $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)**

| PARAMETER | | SN74AHC158 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

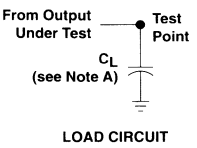
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

PRODUCT PREVIEW

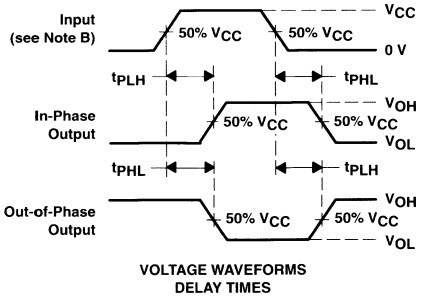
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 20 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

SCLS348C – MAY 1996 – REVISED APRIL 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

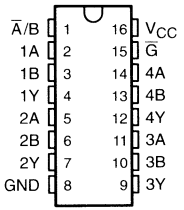
## description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V $V_{CC}$ operation.

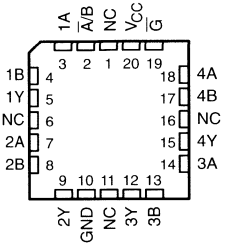
The 'AHCT158 feature a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide inverted data.

The SN54AHCT158 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT158 is characterized for operation from –40°C to 85°C.

**SN54AHCT158 . . . J OR W PACKAGE**
**SN74AHCT158 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT158 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

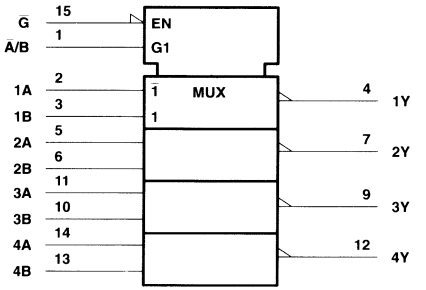
**FUNCTION TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{G}$ | Ā/B | A | B | Y |
| H | X | X | X | H |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

PRODUCT PREVIEW

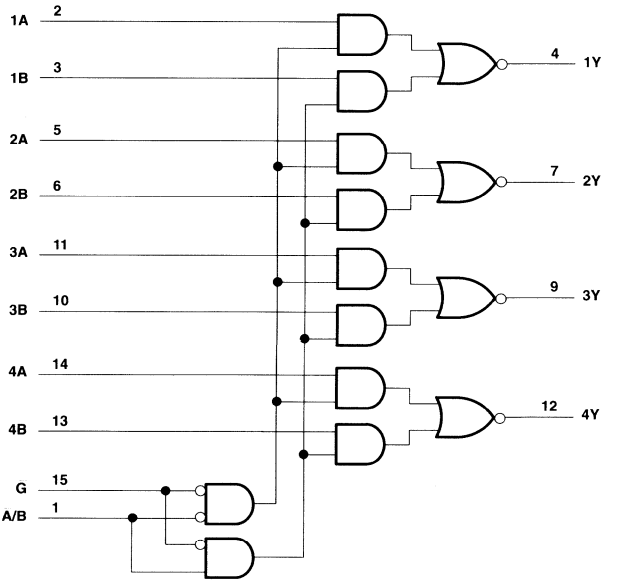
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
N package . . . . . 78°C/W
PW package . . . . . 149°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT158 | | SN74AHCT158 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall time | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT158 | | SN74AHCT158 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4.5 | | | | | | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT158 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$* | A/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | G | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | A/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PLH}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | G | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT158 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | G | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PLH}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |

### noise characteristics $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

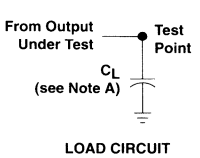
| PARAMETER | | SN74AHCT158 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

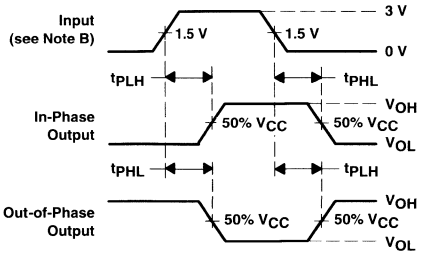
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 26 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

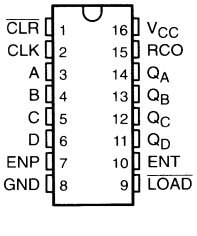
**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

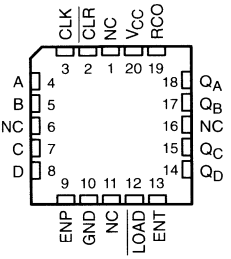
SCLS367A – MAY 1997 – REVISED JUNE 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC161 . . . J OR W PACKAGE**
**SN74AHC161 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC161 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'AHC161 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'AHC161 is asynchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ($\overline{LOAD}$), or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry output (RCO). Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with $Q_A$ high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

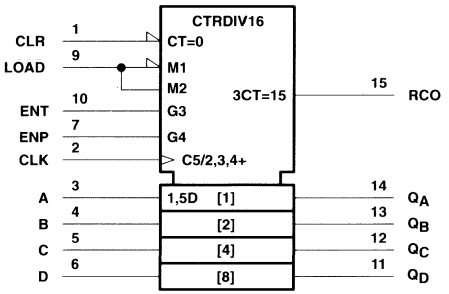
PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

## description (continued)

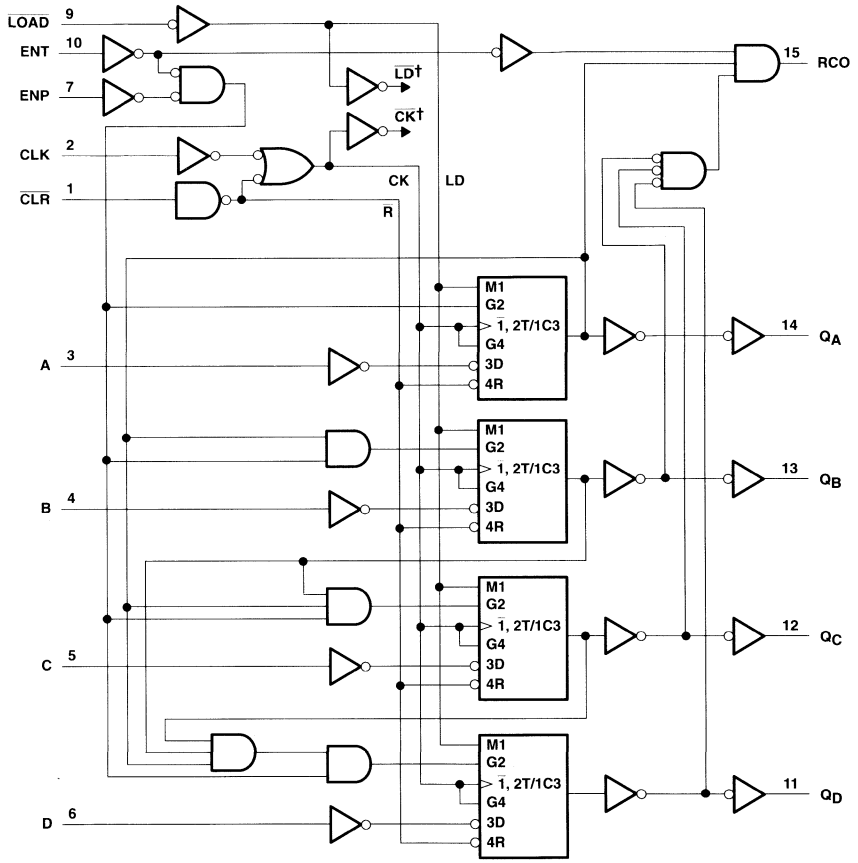
The SN54AHC161 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC161 is characterized for operation from –40°C to 85°C.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)

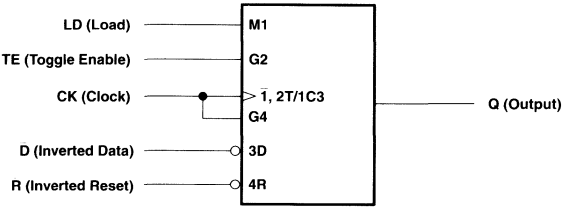



† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

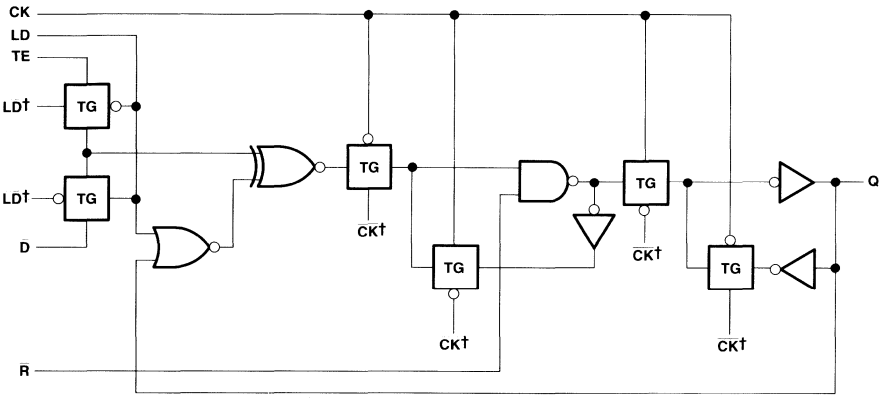
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

### logic symbol, each D/T flip-flop




### logic diagram, each D/T flip-flop (positive logic)

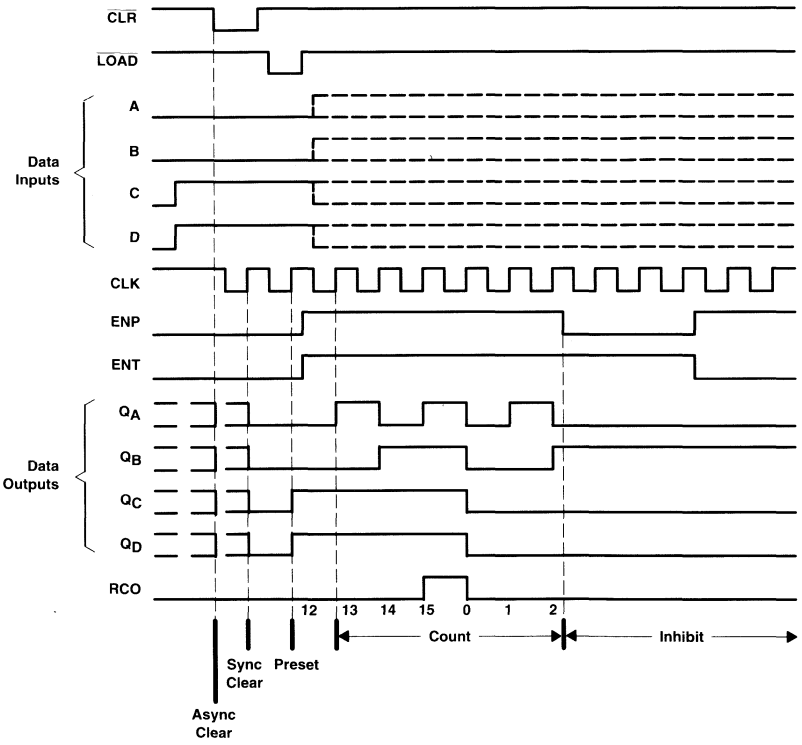



† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

### typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



### absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

### recommended operating conditions (see Note 3)

| | | | SN54AHC161 | | SN74AHC161 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | – 40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC161 | | SN74AHC161 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | | 5 V | | 2 | 10 | | | | 10 | pF |

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHC161 | | SN74AHC161 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | CLK high or low | 5 | | 5 | | 5 | | ns |
| | | $\overline{CLR}$ low | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time before CLK↑ | $\overline{CLR}$ | 2.5 | | 2.5 | | 2.5 | | ns |
| | | Data (A, B, C, and D) | 5.5 | | 6.5 | | 6.5 | | |
| | | ENP, ENT | 7.5 | | 9 | | 9 | | |
| | | $\overline{LOAD}$ low | 8 | | 9.5 | | 9.5 | | |
| $t_h$ | Hold time, all synchronous inputs after CLK↑ | | 1 | | 1 | | 1 | | ns |

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHC161 | | SN74AHC161 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | CLK high or low | 5 | | 5 | | 5 | | ns |
| | | $\overline{CLR}$ low | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time before CLK↑ | $\overline{CLR}$ | 1.5 | | 1.5 | | 1.5 | | ns |
| | | Data (A, B, C, and D) | 4.5 | | 4.5 | | 4.5 | | |
| | | ENP, ENT | 5 | | 6 | | 6 | | |
| | | $\overline{LOAD}$ low | 5 | | 6 | | 6 | | |
| $t_h$ | Hold time, all synchronous inputs after CLK↑ | | 1 | | 1 | | 1 | | ns |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC161 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | | 130 | 80 | | 70 | MHz |
| | | | $C_L$ = 50 pF | | 85 | 55 | | 50 | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 8.3 | 12.8 | 1 | 15 | ns |
| $t_{PHL}$* | | | | | 8.3 | 12.8 | 1 | 15 | |
| $t_{PLH}$* | CLK | RCO (count mode) | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PHL}$* | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PLH}$* | CLK | RCO (preset mode) | $C_L$ = 15 pF | | 11 | 17.2 | 1 | 20 | ns |
| $t_{PHL}$* | | | | | 11 | 17.2 | 1 | 20 | |
| $t_{PLH}$* | ENT | RCO | $C_L$ = 15 pF | | 7.5 | 12.3 | 1 | 14.5 | ns |
| $t_{PHL}$* | | | | | 7.5 | 12.3 | 1 | 14.5 | |
| $t_{PHL}$* | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 8.9 | 13.6 | 1 | 16 | ns |
| | | RCO | | | 8.4 | 13.2 | 1 | 15.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 10.8 | 16.3 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.8 | 16.3 | 1 | 18.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 50 pF | | 13.5 | 20.7 | 1 | 23.5 | ns |
| $t_{PHL}$ | | | | | 13.5 | 20.7 | 1 | 23.5 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 50 pF | | 10.5 | 15.8 | 1 | 18 | ns |
| $t_{PHL}$ | | | | | 10.5 | 15.8 | 1 | 18 | |
| $t_{PHL}$ | CLR | Q | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| | | RCO | | | 10.9 | 16.7 | 1 | 19 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC161 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | | 130 | 80 | | 70 | MHz |
| | | | $C_L$ = 50 pF | | 85 | 55 | | 50 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 8.3 | 12.8 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.3 | 12.8 | 1 | 15 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 15 pF | | 11 | 17.2 | 1 | 20 | ns |
| $t_{PHL}$ | | | | | 11 | 17.2 | 1 | 20 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 15 pF | | 7.5 | 12.3 | 1 | 14.5 | ns |
| $t_{PHL}$ | | | | | 7.5 | 12.3 | 1 | 14.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 8.9 | 13.6 | 1 | 16 | ns |
| | | RCO | | | 8.4 | 13.2 | 1 | 15.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 10.8 | 16.3 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.8 | 16.3 | 1 | 18.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 50 pF | | 13.5 | 20.7 | 1 | 23.5 | ns |
| $t_{PHL}$ | | | | | 13.5 | 20.7 | 1 | 23.5 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 50 pF | | 10.5 | 15.8 | 1 | 18 | ns |
| $t_{PHL}$ | | | | | 10.5 | 15.8 | 1 | 18 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| | | RCO | | | 10.9 | 16.7 | 1 | 19 | |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC161 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | | 185 | 135 | | 115 | MHz |
| | | | $C_L$ = 50 pF | | 125 | 95 | | 85 | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | CLK | RCO (count mode) | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | CLK | RCO (preset mode) | $C_L$ = 15 pF | | 6.2 | 10.3 | 1 | 12 | ns |
| $t_{PHL}$* | | | | | 6.2 | 10.3 | 1 | 12 | |
| $t_{PLH}$* | ENT | RCO | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PHL}$* | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 5.5 | 9 | 1 | 10.5 | ns |
| | | RCO | | | 5 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 50 pF | | 7.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 7.7 | 12.3 | 1 | 14 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 7 | 11 | 1 | 12.5 | ns |
| | | RCO | | | 6.5 | 10.6 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC161 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | | 185 | 135 | | 115 | MHz |
| | | | $C_L$ = 50 pF | | 125 | 95 | | 85 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 15 pF | | 6.2 | 10.3 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 6.2 | 10.3 | 1 | 12 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 5.5 | 9 | 1 | 10.5 | ns |
| | | RCO | | | 5 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 50 pF | | 7.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 7.7 | 12.3 | 1 | 14 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 7 | 11 | 1 | 12.5 | ns |
| | | RCO | | | 6.5 | 10.6 | 1 | 12 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

| PARAMETER | | SN74AHC161 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

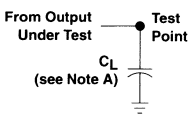
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

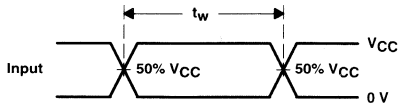
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 23 | pF |

PRODUCT PREVIEW

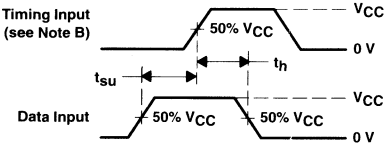
## PARAMETER MEASUREMENT INFORMATION



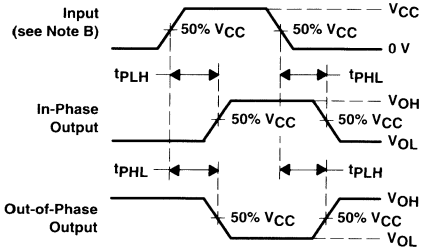

LOAD CIRCUIT




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES

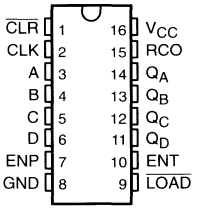
NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

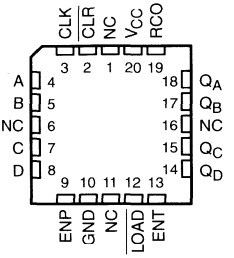
SCLS368A – MAY 1997 – REVISED JUNE 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT161 . . . J OR W PACKAGE**
**SN74AHCT161 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT161 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'AHCT161 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'AHCT161 is asynchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ($\overline{LOAD}$), or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry (RCO) output. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with $Q_A$ high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

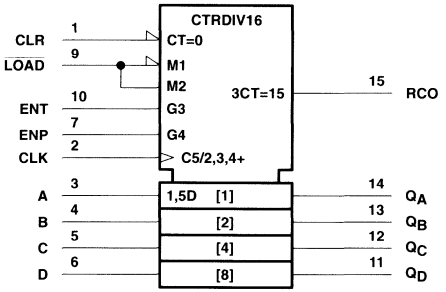
PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

## description (continued)

The SN54AHCT161 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT161 is characterized for operation from –40°C to 85°C.

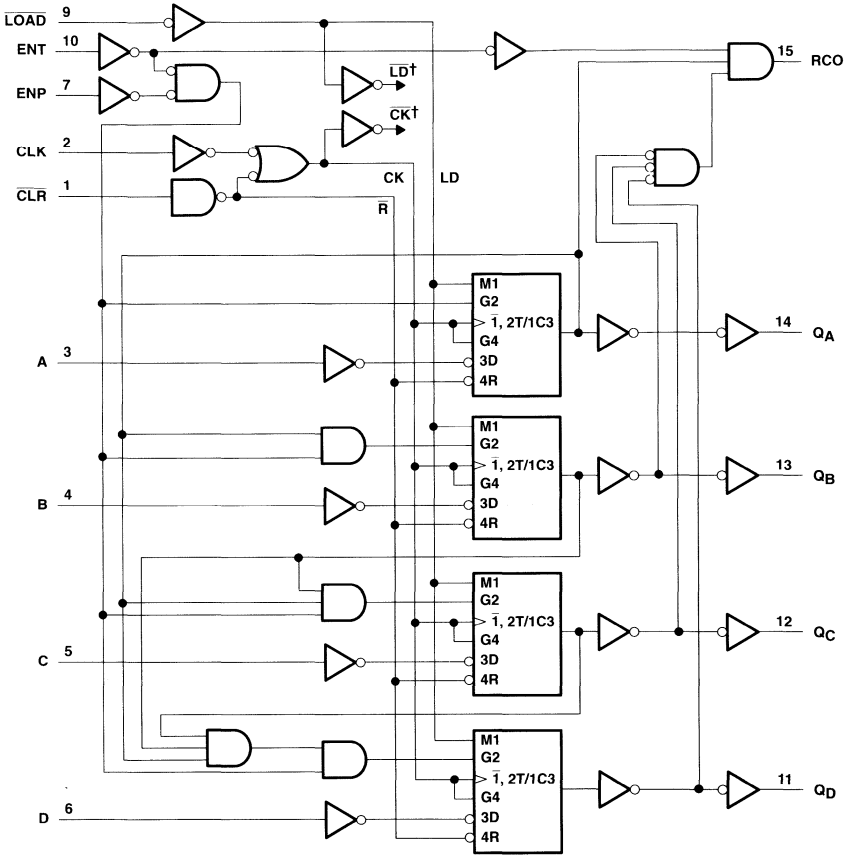
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

## logic diagram (positive logic)

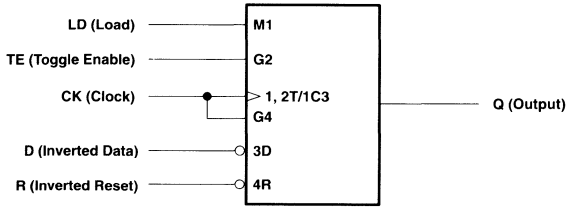



† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

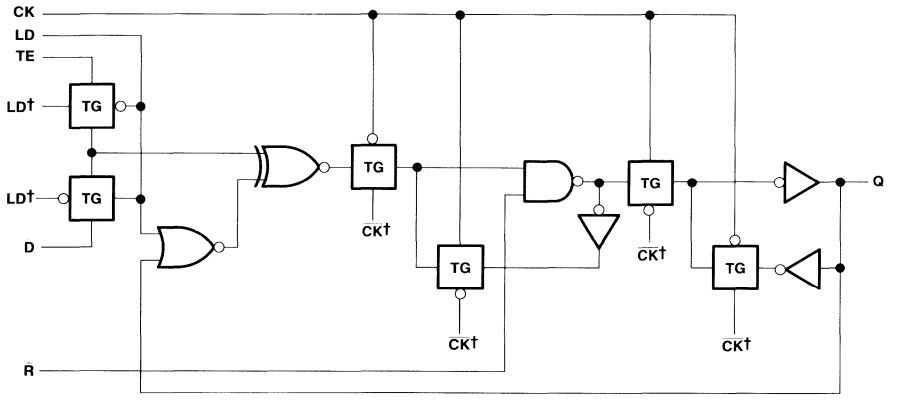
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

## logic symbol, each D/T flip-flop




## logic diagram, each D/T flip-flop (positive logic)



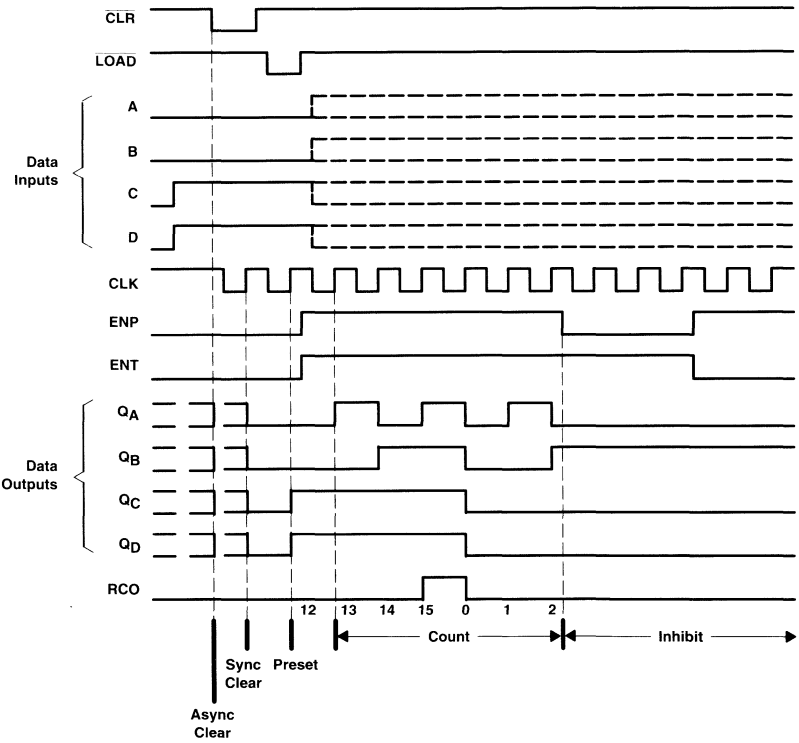

† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

PRODUCT PREVIEW

### typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



## absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

## recommended operating conditions (see Note 3)

| | | SN54AHCT161 | | SN74AHCT161 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT161 | | SN74AHCT161 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHCT161 | | SN74AHCT161 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | CLK high or low | 5 | | 5 | | 5 | | ns |
| | | $\overline{CLR}$ low | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time before CLK↑ | CLR | 1.5 | | 1.5 | | 1.5 | | ns |
| | | Data (A, B, C, and D) | 4.5 | | 4.5 | | 4.5 | | |
| | | ENP, ENT | 5 | | 6 | | 6 | | |
| | | $\overline{LOAD}$ low | 5 | | 6 | | 6 | | |
| $t_h$ | Hold time, all synchronous inputs after CLK↑ | | 1 | | 1 | | 1 | | ns |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT161 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | | 185 | 135 | | 115 | MHz |
| | | | $C_L$ = 50 pF | | 125 | 95 | | 85 | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | CLK | RCO (count mode) | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | CLK | RCO (preset mode) | $C_L$ = 15 pF | | 6.2 | 10.3 | 1 | 12 | ns |
| $t_{PHL}$* | | | | | 6.2 | 10.3 | 1 | 12 | |
| $t_{PLH}$* | ENT | RCO | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PHL}$* | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 5.5 | 9 | 1 | 10.5 | ns |
| | | RCO | | | 5 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 50 pF | | 7.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 7.7 | 12.3 | 1 | 14 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 7 | 11 | 1 | 12.5 | ns |
| | | RCO | | | 6.5 | 10.6 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT161 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | | 185 | 135 | | 115 | MHz |
| | | | $C_L$ = 50 pF | | 125 | 95 | | 85 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 15 pF | | 6.2 | 10.3 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 6.2 | 10.3 | 1 | 12 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 5.5 | 9 | 1 | 10.5 | ns |
| | | RCO | | | 5 | 8.6 | 1 | 10 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 50 pF | | 7.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 7.7 | 12.3 | 1 | 14 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 7 | 11 | 1 | 12.5 | ns |
| | | RCO | | | 6.5 | 10.6 | 1 | 12 | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

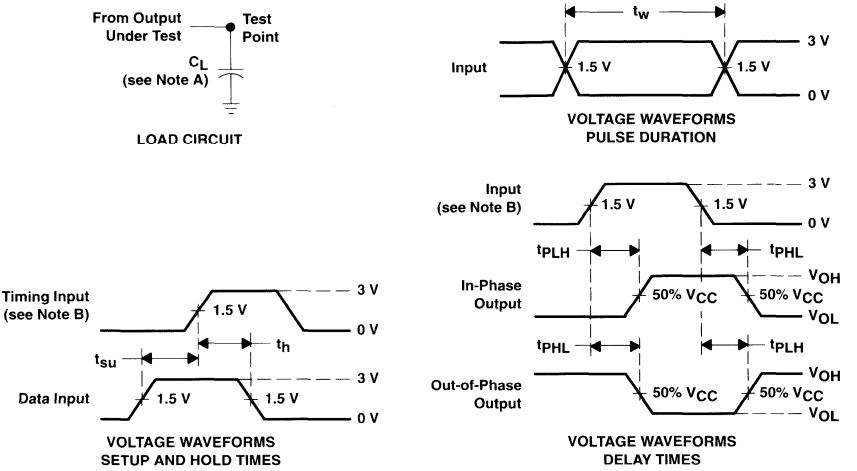
| PARAMETER | | SN74AHCT161 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 23 | pF |

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

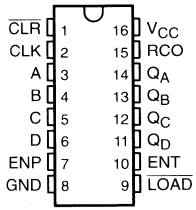
**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

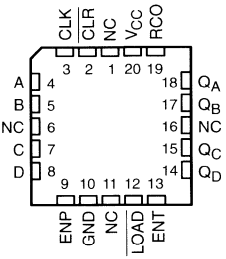
SCLS369A – MAY 1997 – REVISED JUNE 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC163 . . . J OR W PACKAGE**
**SN74AHC163 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC163 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'AHC163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'AHC163 is synchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{CLR}$ to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with $Q_A$ high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

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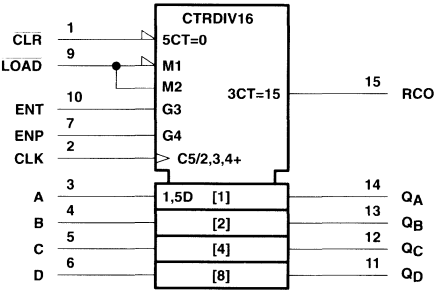
EPIC is a trademark of Texas Instruments Incorporated.

## description (continued)

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

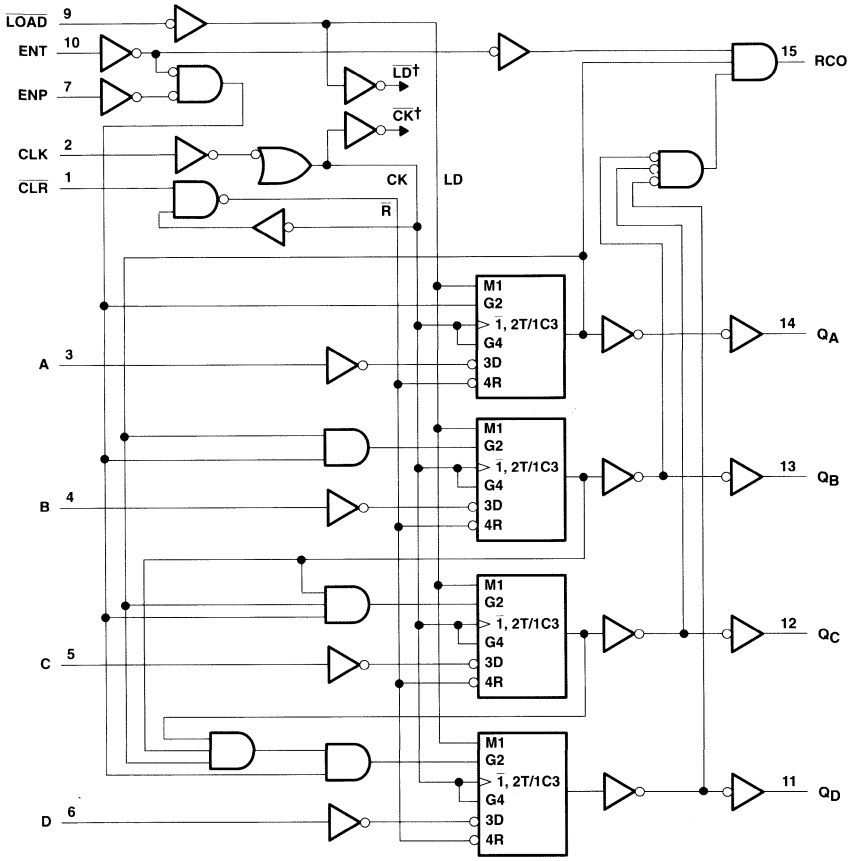
The SN54AHC163 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC163 is characterized for operation from –40°C to 85°C.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)

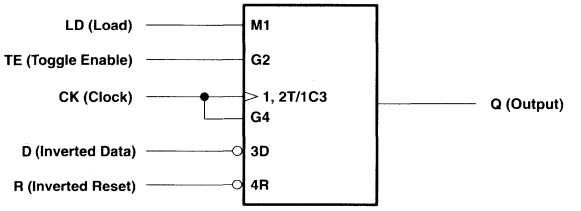



† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

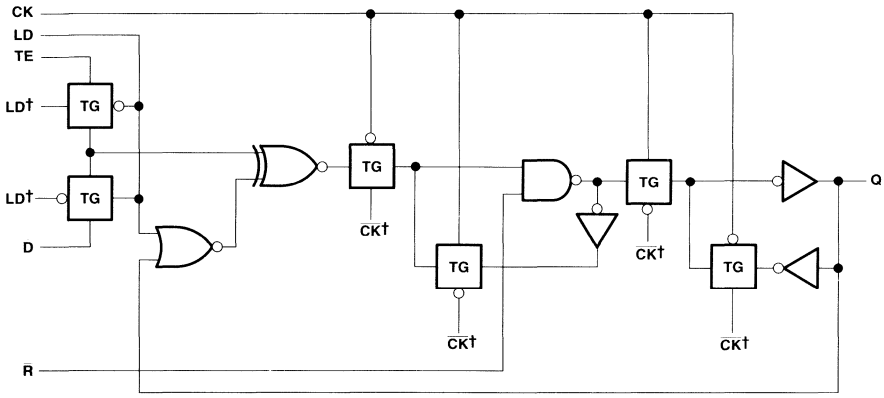
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

### logic symbol, each D/T flip-flop




### logic diagram, each D/T flip-flop (positive logic)

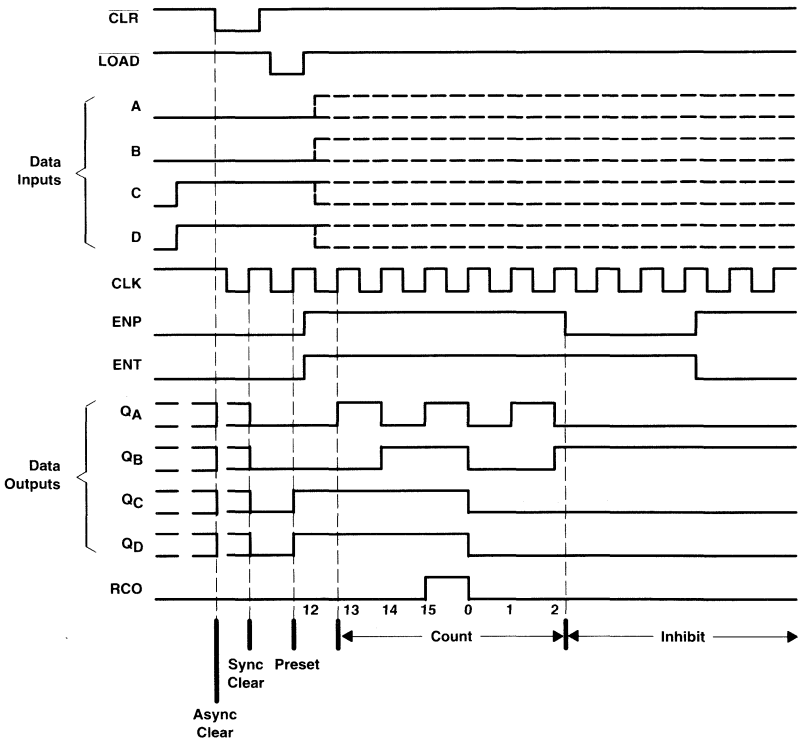



† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

## typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



### absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

### recommended operating conditions (see Note 3)

| | | | SN54AHC163 | | SN74AHC163 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | – 40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC163 | | SN74AHC163 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHC163 | | SN74AHC163 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time before CLK↑ | $\overline{CLR}$ | 4 | | 4 | | 4 | | ns |
| | | Data (A, B, C, and D) | 5.5 | | 6.5 | | 6.5 | | |
| | | ENP, ENT | 7.5 | | 9 | | 9 | | |
| | | $\overline{LOAD}$ low | 8 | | 9.5 | | 9.5 | | |
| $t_h$ | Hold time, all synchronous inputs after CLK↑ | | 1 | | 1 | | 1 | | ns |

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHC163 | | SN74AHC163 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time before CLK↑ | $\overline{CLR}$ | 3.5 | | 3.5 | | 3.5 | | ns |
| | | Data (A, B, C, and D) | 4.5 | | 4.5 | | 4.5 | | |
| | | ENP, ENT | 5 | | 6 | | 6 | | |
| | | $\overline{LOAD}$ low | 5 | | 6 | | 6 | | |
| $t_h$ | Hold time, all synchronous inputs after CLK↑ | | 1 | | 1 | | 1 | | ns |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC163 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | | 130 | 80 | | 70 | MHz |
| | | | $C_L$ = 50 pF | | 85 | 55 | | 50 | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 8.3 | 12.8 | 1 | 15 | ns |
| $t_{PHL}$* | | | | | 8.3 | 12.8 | 1 | 15 | |
| $t_{PLH}$* | CLK | RCO (count mode) | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PHL}$* | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PLH}$* | CLK | RCO (preset mode) | $C_L$ = 15 pF | | 11 | 17.2 | 1 | 20 | ns |
| $t_{PHL}$* | | | | | 11 | 17.2 | 1 | 20 | |
| $t_{PLH}$* | ENT | RCO | $C_L$ = 15 pF | | 7.5 | 12.3 | 1 | 14.5 | ns |
| $t_{PHL}$* | | | | | 7.5 | 12.3 | 1 | 14.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 10.8 | 16.3 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.8 | 16.3 | 1 | 18.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 50 pF | | 13.5 | 20.7 | 1 | 23.5 | ns |
| $t_{PHL}$ | | | | | 13.5 | 20.7 | 1 | 23.5 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 50 pF | | 10.5 | 15.8 | 1 | 18 | ns |
| $t_{PHL}$ | | | | | 10.5 | 15.8 | 1 | 18 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC163 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | | 130 | 80 | | 70 | MHz |
| | | | $C_L$ = 50 pF | | 85 | 55 | | 50 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 8.3 | 12.8 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.3 | 12.8 | 1 | 15 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 15 pF | | 11 | 17.2 | 1 | 20 | ns |
| $t_{PHL}$ | | | | | 11 | 17.2 | 1 | 20 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 15 pF | | 7.5 | 12.3 | 1 | 14.5 | ns |
| $t_{PHL}$ | | | | | 7.5 | 12.3 | 1 | 14.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 10.8 | 16.3 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.8 | 16.3 | 1 | 18.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 50 pF | | 13.5 | 20.7 | 1 | 23.5 | ns |
| $t_{PHL}$ | | | | | 13.5 | 20.7 | 1 | 23.5 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 50 pF | | 10.5 | 15.8 | 1 | 18 | ns |
| $t_{PHL}$ | | | | | 10.5 | 15.8 | 1 | 18 | |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC163 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | | 185 | 135 | | 115 | MHz |
| | | | $C_L$ = 50 pF | | 125 | 95 | | 85 | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | CLK | RCO (count mode) | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | CLK | RCO (preset mode) | $C_L$ = 15 pF | | 6.2 | 10.3 | 1 | 12 | ns |
| $t_{PHL}$* | | | | | 6.2 | 10.3 | 1 | 12 | |
| $t_{PLH}$* | ENT | RCO | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 50 pF | | 7.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 7.7 | 12.3 | 1 | 14 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC163 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX |
| | | | | MIN | TYP | MAX | | |
| $f_{max}$ | | | $C_L$ = 15 pF | | 185 | 135 | | 115 | MHz |
| | | | $C_L$ = 50 pF | | 125 | 95 | | 85 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 15 pF | | 6.2 | 10.3 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 6.2 | 10.3 | 1 | 12 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 50 pF | | 7.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 7.7 | 12.3 | 1 | 14 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

| PARAMETER | | SN74AHC163 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

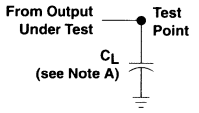
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

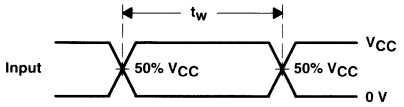
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 23 | pF |

PRODUCT PREVIEW

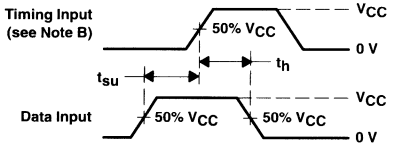
## PARAMETER MEASUREMENT INFORMATION



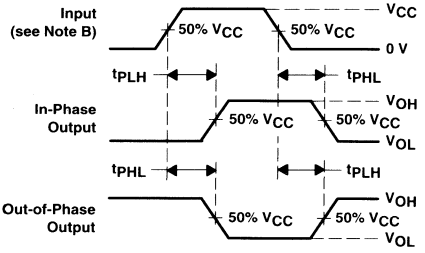

LOAD CIRCUIT




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES

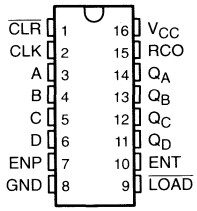
NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

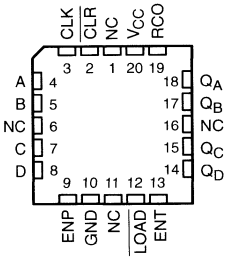
SCLS370A – MAY 1997 – REVISED JUNE 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT163 . . . J OR W PACKAGE**
**SN74AHCT163 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT163 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'AHCT163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'AHCT163 is synchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{CLR}$ to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with $Q_A$ high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

PRODUCT PREVIEW

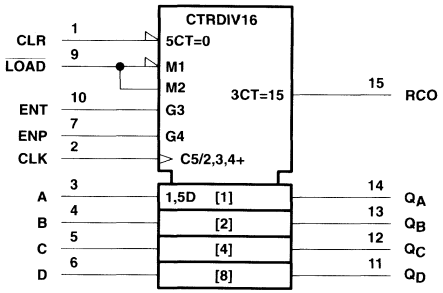
EPIC is a trademark of Texas Instruments Incorporated.

## description (continued)

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The SN54AHCT163 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT163 is characterized for operation from –40°C to 85°C.

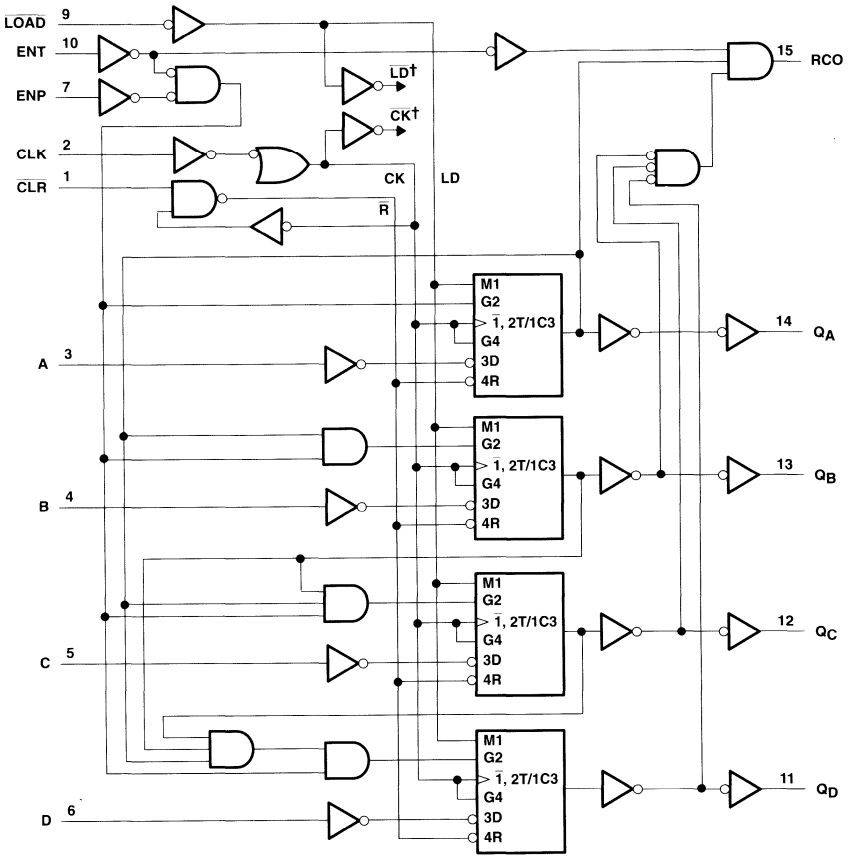
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

## logic diagram (positive logic)

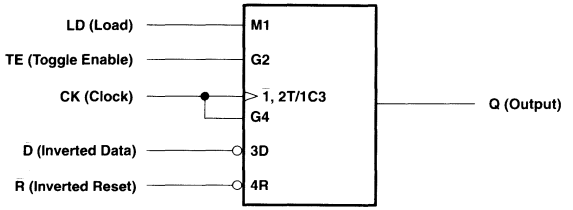



† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

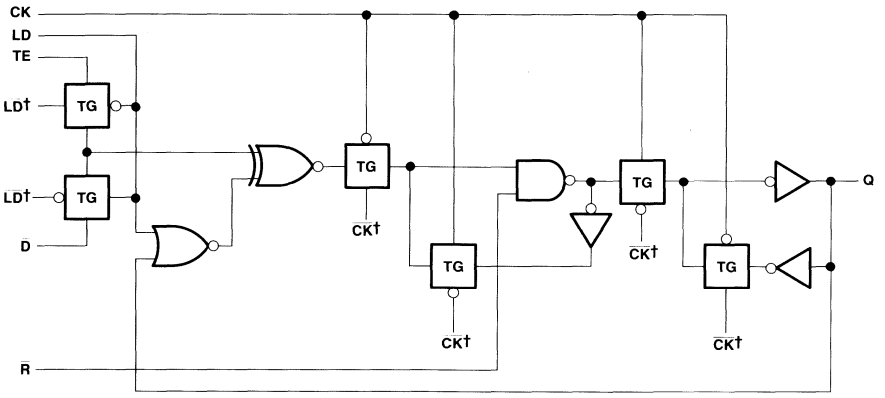
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

### logic symbol, each D/T flip-flop




### logic diagram, each D/T flip-flop (positive logic)

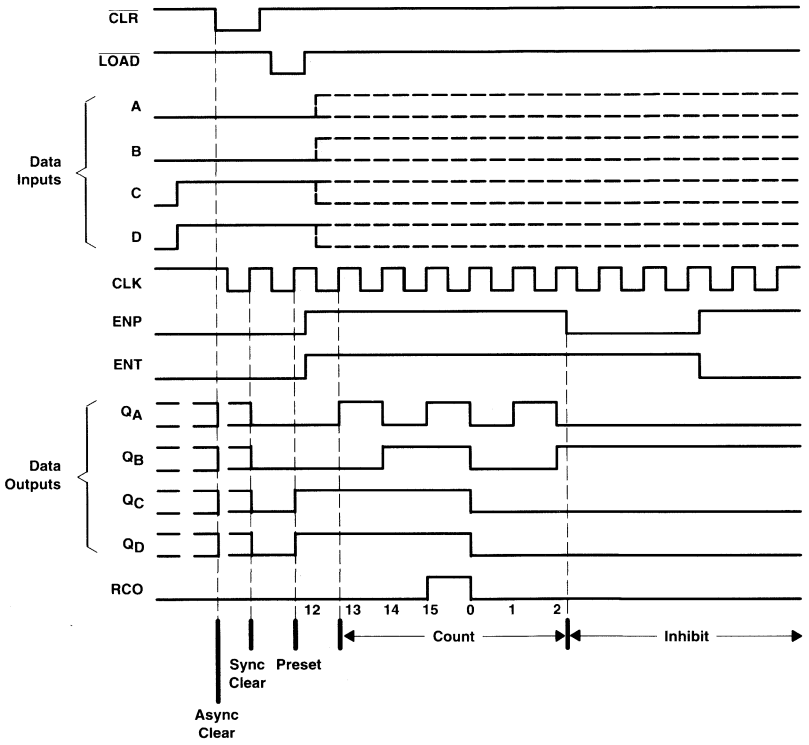



† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

### typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



### absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

### recommended operating conditions (see Note 3)

| | | SN54AHCT163 | | SN74AHCT163 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT163 | | SN74AHCT163 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | µA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| | | | $T_A$ = 25°C | | SN54AHCT163 | | SN74AHCT163 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time before CLK↑ | $\overline{CLR}$ | 3.5 | | 3.5 | | 3.5 | | ns |
| | | Data (A, B, C, and D) | 4.5 | | 4.5 | | 4.5 | | |
| | | ENP, ENT | 5 | | 6 | | 6 | | |
| | | $\overline{LOAD}$ low | 5 | | 6 | | 6 | | |
| $t_h$ | Hold time, all synchronous inputs after CLK↑ | | 1 | | 1 | | 1 | | ns |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT163 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | | 185 | 135 | | 115 | MHz |
| | | | $C_L$ = 50 pF | | 125 | 95 | | 85 | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | CLK | RCO (count mode) | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$* | CLK | RCO (preset mode) | $C_L$ = 15 pF | | 6.2 | 10.3 | 1 | 12 | ns |
| $t_{PHL}$* | | | | | 6.2 | 10.3 | 1 | 12 | |
| $t_{PLH}$* | ENT | RCO | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 50 pF | | 7.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 7.7 | 12.3 | 1 | 14 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT163 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | | 185 | 135 | | 115 | MHz |
| | | | $C_L$ = 50 pF | | 125 | 95 | | 85 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 15 pF | | 6.2 | 10.3 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 6.2 | 10.3 | 1 | 12 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 15 pF | | 4.9 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 8.1 | 1 | 9.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (count mode) | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | RCO (preset mode) | $C_L$ = 50 pF | | 7.7 | 12.3 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 7.7 | 12.3 | 1 | 14 | |
| $t_{PLH}$ | ENT | RCO | $C_L$ = 50 pF | | 6.4 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.1 | 1 | 11.5 | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

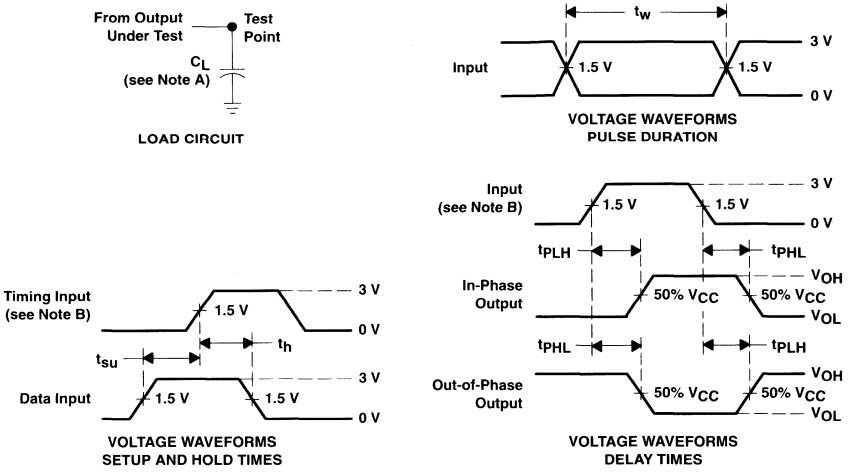
| PARAMETER | | SN74AHCT163 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 23 | pF |

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

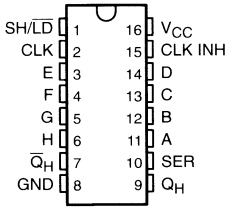
**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

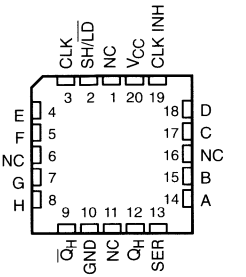
SCLS371 – MAY 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC165 . . . J OR W PACKAGE**
**SN74AHC165 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC165 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC165 are 8-bit parallel-load shift registers that, when clocked, shift the data toward a serial ($Q_H$) output. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The 'AHC165 also feature a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}_H$) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. While SH/$\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

The SN54AHC165 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC165 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

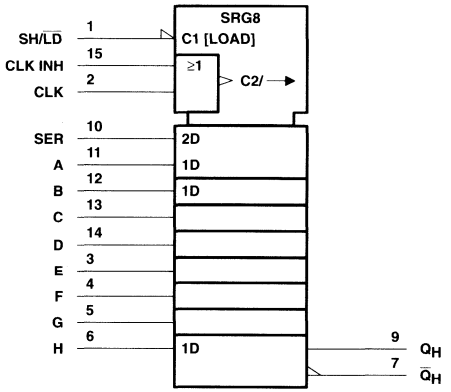
EPIC is a trademark of Texas Instruments Incorporated.

**FUNCTION TABLE**

| INPUTS | | | FUNCTION |
|---|---|---|---|
| SH/$\overline{LD}$ | CLK | CLK INH | |
| L | X | X | Parallel load |
| H | H | X | No change |
| H | X | H | No change |
| H | L | ↑ | Shift† |
| H | ↑ | L | Shift† |

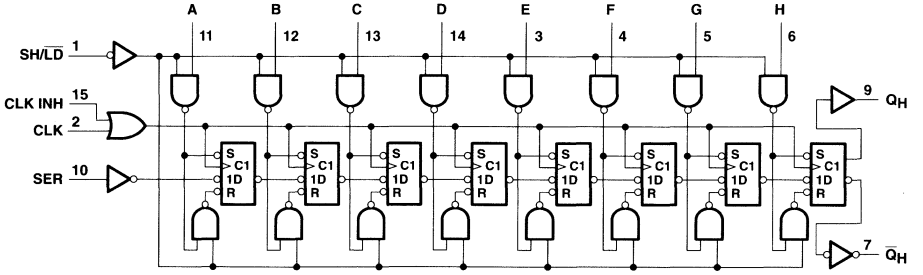
† Shift = content of each internal register shifts toward serial output $Q_H$. Data at SER is shifted into the first register.

## logic symbol†



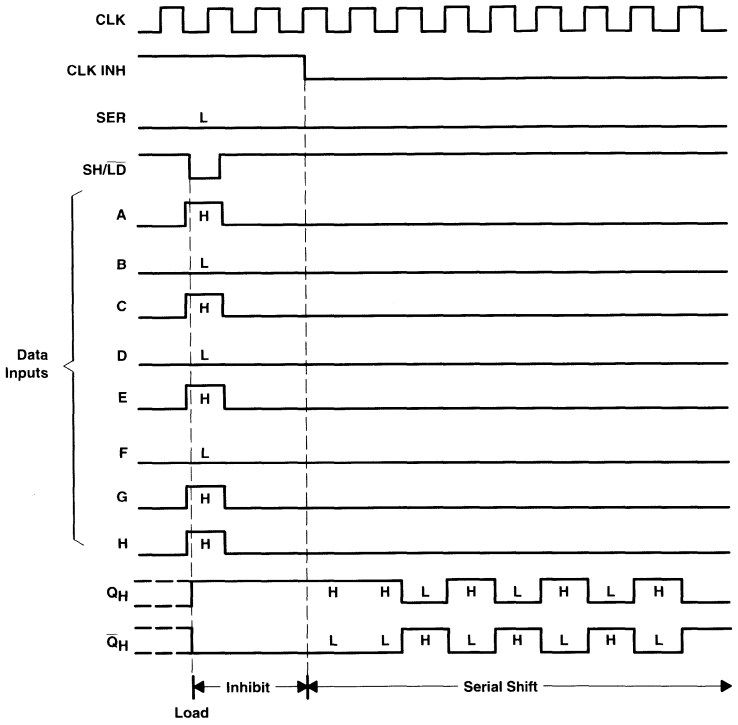

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

**typical shift, load, and inhibit sequence**



## absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

## recommended operating conditions (see Note 3)

| | | | SN54AHC165 | | SN74AHC165 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | – 40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC165 | | SN74AHC165 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHC165 | | SN74AHC165 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | CLK high or low | | | | | | | ns |
| | | SH/$\overline{LD}$ low | | | | | | | |
| $t_{su}$ | Setup time | CLK INH high before CLK↑ | | | | | | | ns |
| | | CLK INH low before CLK↑ | | | | | | | |
| | | Data before SH/$\overline{LD}$↓ | | | | | | | |
| | | SER before CLK↑ | | | | | | | |
| | | SH/$\overline{LD}$ high before CLK↑ | | | | | | | |
| $t_h$ | Hold time | SER data after CLK↑ | | | | | | | ns |
| | | PAR data after SH/$\overline{LD}$↓ | | | | | | | |

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHC165 | | SN74AHC165 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | CLK high or low | | | | | | | ns |
| | | SH/$\overline{LD}$ low | | | | | | | |
| $t_{su}$ | Setup time | CLK INH high before CLK↑ | | | | | | | ns |
| | | CLK INH low before CLK↑ | | | | | | | |
| | | Data before SH/$\overline{LD}$↓ | | | | | | | |
| | | SER before CLK↑ | | | | | | | |
| | | SH/$\overline{LD}$ high before CLK↑ | | | | | | | |
| $t_h$ | Hold time | SER data after CLK↑ | | | | | | | ns |
| | | PAR data after SH/$\overline{LD}$↓ | | | | | | | |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC165 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | | | | | | MHz |
| | | | $C_L$ = 50 pF | | | | | | |
| $t_{PLH}$* | SH/$\overline{LD}$ | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$* | | | | | | | | | |
| $t_{PLH}$* | CLK | $Q_H$ or $Q_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$* | | | | | | | | | |
| $t_{PLH}$* | H | $Q_H$ or $Q_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$* | | | | | | | | | |
| $t_{PLH}$ | SH/LD | $Q_H$ or $Q_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | CLK | $Q_H$ or $Q_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | H | $Q_H$ or $Q_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC165 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | | | | | | MHz |
| | | | $C_L$ = 50 pF | | | | | | |
| $t_{PLH}$ | SH/LD | $Q_H$ or $Q_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | CLK | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | H | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | SH/$\overline{LD}$ | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | CLK | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | H | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC165 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | | | | | | MHz |
| | | | $C_L$ = 50 pF | | | | | | |
| $t_{PLH}$* | SH/$\overline{LD}$ | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$* | | | | | | | | | |
| $t_{PLH}$* | CLK | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$* | | | | | | | | | |
| $t_{PLH}$* | H | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$* | | | | | | | | | |
| $t_{PLH}$ | SH/$\overline{LD}$ | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | CLK | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | H | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC165 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | | | | | | MHz |
| | | | $C_L$ = 50 pF | | | | | | |
| $t_{PLH}$ | SH/$\overline{LD}$ | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | CLK | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | H | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | SH/$\overline{LD}$ | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | CLK | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | H | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

| PARAMETER | | SN74AHC165 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

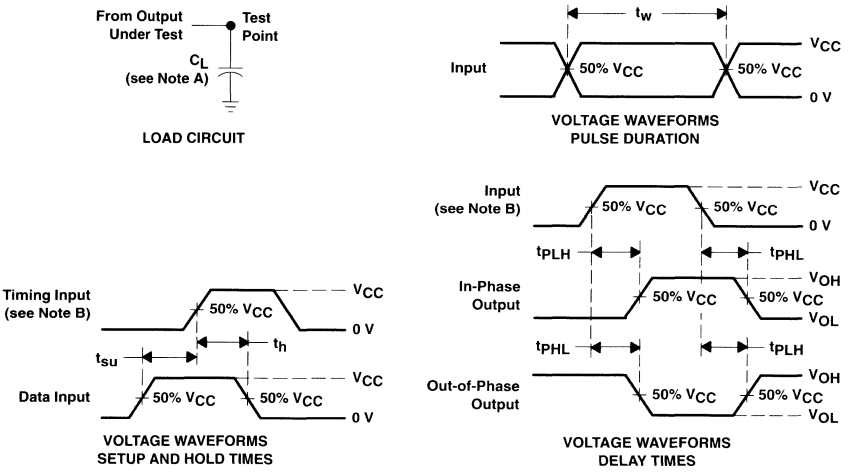
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | | pF |

PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION

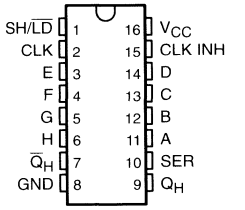



NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

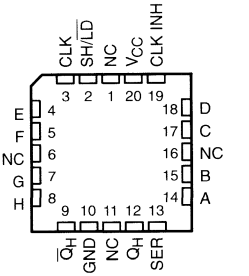
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT165 . . . J OR W PACKAGE**
**SN74AHCT165 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT165 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHCT165 are 8-bit parallel-load shift registers that, when clocked, shift the data toward a serial ($Q_H$) output. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The 'AHCT165 also feature a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}_H$) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. While SH/$\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

The SN54AHCT165 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT165 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

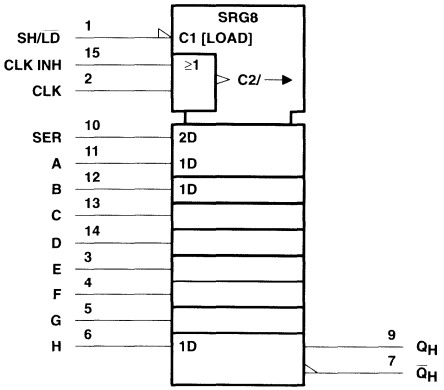
EPIC is a trademark of Texas Instruments Incorporated.

**FUNCTION TABLE**

| INPUTS | | | FUNCTION |
|---|---|---|---|
| SH/$\overline{LD}$ | CLK | CLK INH | |
| L | X | X | Parallel load |
| H | H | X | No change |
| H | X | H | No change |
| H | L | ↑ | Shift† |
| H | ↑ | L | Shift† |

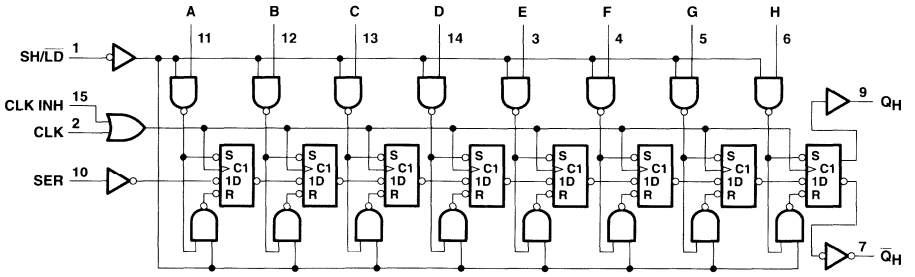
† Shift = content of each internal register shifts toward serial output $Q_H$. Data at SER is shifted into the first register.

## logic symbol†



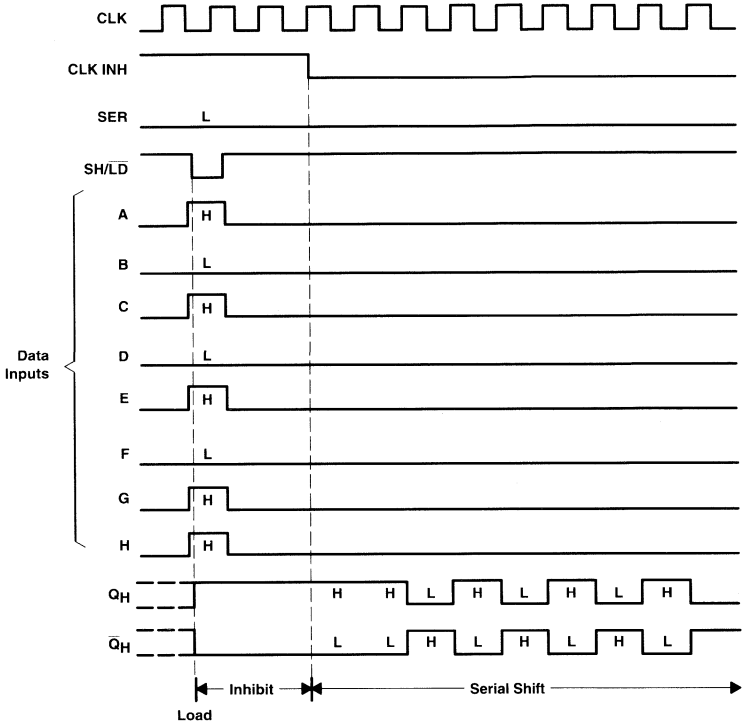

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

**typical shift, load, and inhibit sequence**




PRODUCT PREVIEW

### absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

PRODUCT PREVIEW

### recommended operating conditions (see Note 3)

| | | SN54AHCT165 | | SN74AHCT165 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT165 | | SN74AHCT165 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| | | | $T_A$ = 25°C | | SN54AHCT165 | | SN74AHCT165 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | CLK high or low | | | | | | | ns |
| | | SH/$\overline{LD}$ low | | | | | | | |
| $t_{su}$ | Setup time | CLK INH high before CLK↑ | | | | | | | ns |
| | | CLK INH low before CLK↑ | | | | | | | |
| | | Data before SH/$\overline{LD}$↓ | | | | | | | |
| | | SER before CLK↑ | | | | | | | |
| | | SH/$\overline{LD}$ high before CLK↑ | | | | | | | |
| $t_h$ | Hold time | SER data after CLK↑ | | | | | | | ns |
| | | PAR data after SH/$\overline{LD}$↓ | | | | | | | |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT165 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | | | | | | MHz |
| | | | $C_L$ = 50 pF | | | | | | |
| $t_{PLH}$* | SH/$\overline{LD}$ | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$* | | | | | | | | | |
| $t_{PLH}$* | CLK | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$* | | | | | | | | | |
| $t_{PLH}$* | H | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PHL}$* | | | | | | | | | |
| $t_{PLH}$ | SH/$\overline{LD}$ | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | CLK | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | H | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | | ns |
| $t_{PHL}$ | | | | | | | | | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT165 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN MAX | |
| | | | | MIN | TYP | MAX | | |
| $f_{max}$ | | | $C_L$ = 15 pF | | | | | MHz |
| | | | $C_L$ = 50 pF | | | | | |
| $t_{PLH}$ | SH/$\overline{LD}$ | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 15 pF | | | | | ns |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | CLK | $Q_H$ or $Q_H$ | $C_L$ = 15 pF | | | | | ns |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | H | $Q_H$ or $Q_H$ | $C_L$ = 15 pF | | | | | ns |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | SH/LD | $Q_H$ or $Q_H$ | $C_L$ = 50 pF | | | | | ns |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | CLK | $Q_H$ or $Q_H$ | $C_L$ = 50 pF | | | | | ns |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | H | $Q_H$ or $\overline{Q}_H$ | $C_L$ = 50 pF | | | | | ns |
| $t_{PHL}$ | | | | | | | | |

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

| PARAMETER | | SN74AHCT165 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.4 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

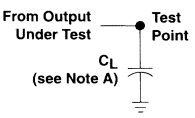
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

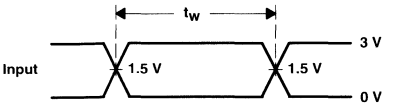
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | | pF |

PRODUCT PREVIEW

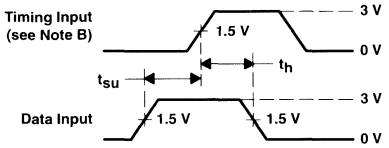
## PARAMETER MEASUREMENT INFORMATION



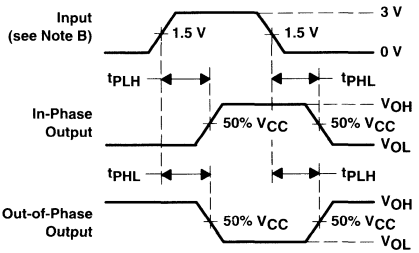

LOAD CIRCUIT




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES

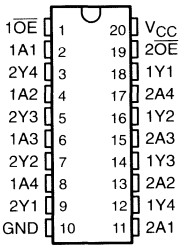
NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

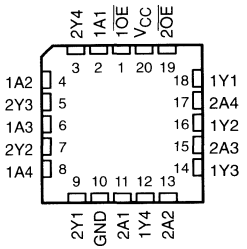
PRODUCT PREVIEW

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC240 . . . J OR W PACKAGE**
**SN74AHC240 . . . DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC240 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'AHC240 are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

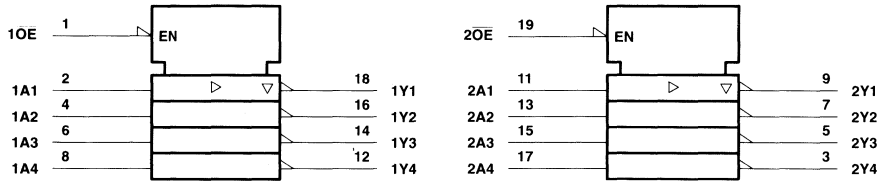
The SN54AHC240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC240 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

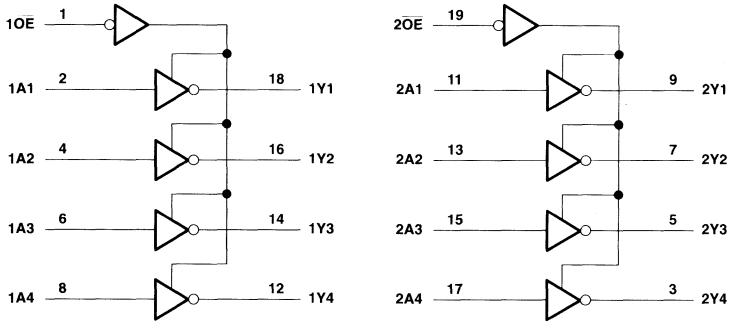
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I < 0$) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC240 | | SN74AHC240 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC240 | | SN74AHC240 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | Data inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| | Control inputs | | | | | ±0.1 | | ±1 | | ±1 | |
| $I_{OZ}$† | | $V_O$ = $V_{CC}$ or GND, $V_I$ ($\overline{OE}$) = $V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_o$ | | $V_O$ = $V_{CC}$ or GND | 5 V | | 3.5 | | | | | | pF |

† The parameter $I_{OZ}$ includes the input leakage current.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC240 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5.3 | 7.5 | 1 | 9 | ns |
| $t_{PHL}$* | | | | | 5.3 | 7.5 | 1 | 9 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6.6 | 10.6 | 1 | 12.5 | ns |
| $t_{PZL}$* | | | | | 6.6 | 10.6 | 1 | 12.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7.8 | 11.5 | 1 | 12.5 | ns |
| $t_{PLZ}$* | | | | | 7.8 | 11.5 | 1 | 12.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.8 | 11 | 1 | 12.5 | ns |
| $t_{PHL}$ | | | | | 7.8 | 11 | 1 | 12.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 9.1 | 14.1 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 9.1 | 14.1 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 10.3 | 14 | 1 | 16 | ns |
| $t_{PLZ}$ | | | | | 10.3 | 14 | 1 | 16 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC240 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5.3 | 7.5 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 9 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6.6 | 10.6 | 1 | 12.5 | ns |
| $t_{PZL}$ | | | | | 6.6 | 10.6 | 1 | 12.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7.8 | 11.5 | 1 | 12.5 | ns |
| $t_{PLZ}$ | | | | | 7.8 | 11.5 | 1 | 12.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.8 | 11 | 1 | 12.5 | ns |
| $t_{PHL}$ | | | | | 7.8 | 11 | 1 | 12.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 9.1 | 14.1 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 9.1 | 14.1 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 10.3 | 14 | 1 | 16 | ns |
| $t_{PLZ}$ | | | | | 10.3 | 14 | 1 | 16 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC240 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.6 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.6 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.7 | 7.3 | 1 | 8.5 | ns |
| $t_{PZL}$* | | | | | 4.7 | 7.3 | 1 | 8.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.2 | 7.2 | 1 | 8.5 | ns |
| $t_{PLZ}$* | | | | | 5.2 | 7.2 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.1 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.1 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 9.3 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 6.2 | 9.3 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.7 | 9.2 | 1 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 6.7 | 9.2 | 1 | 10.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC240 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.6 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.6 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.7 | 7.3 | 1 | 8.5 | ns |
| $t_{PZL}$ | | | | | 4.7 | 7.3 | 1 | 8.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.2 | 7.2 | 1 | 8.5 | ns |
| $t_{PLZ}$ | | | | | 5.2 | 7.2 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.1 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.1 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 9.3 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 6.2 | 9.3 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.7 | 9.2 | 1 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 6.7 | 9.2 | 1 | 10.5 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC240 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

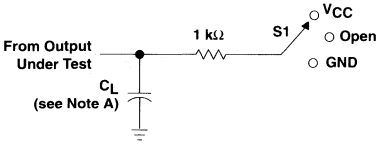
| PARAMETER | | SN74AHC240 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.6 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.6 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.6 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

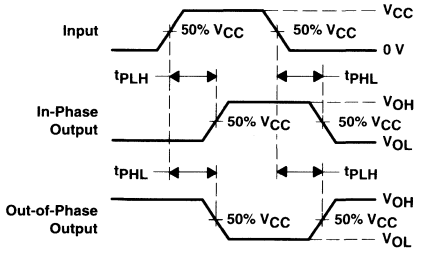
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 10 | pF |

## PARAMETER MEASUREMENT INFORMATION

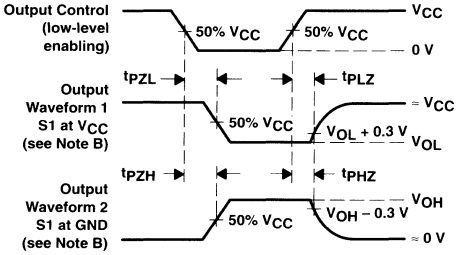



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



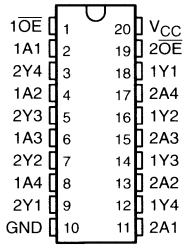

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

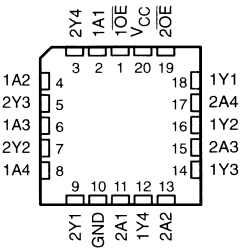
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

**SN54AHCT240 . . . J OR W PACKAGE**
**SN74AHCT240 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT240 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'AHCT240 are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

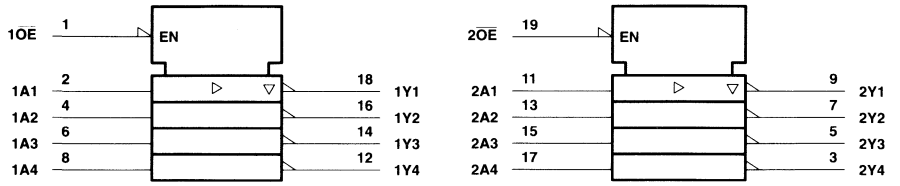
The SN54AHCT240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT240 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each buffer/driver)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

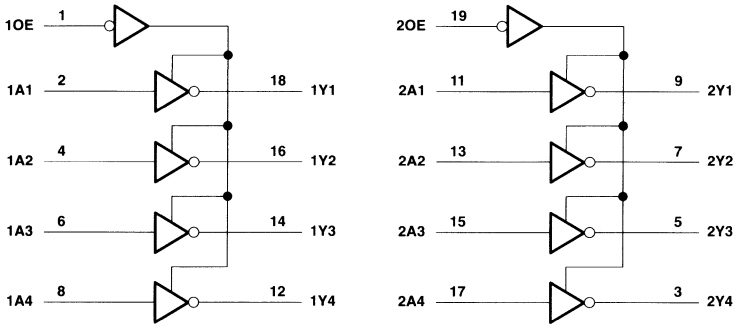
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$ (see Note 1) | –0.5 V to 7 V |
| Output voltage range, $V_O$ (see Note 1) | –0.5 V to $V_{CC}$ + 0.5 V |
| Input clamp current, $I_{IK}$ ($V_I$ < 0) | –20 mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) | ±20 mA |
| Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) | ±25 mA |
| Continuous current through $V_{CC}$ or GND | ±75 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package | 115°C/W |
| DGV package | 146°C/W |
| DW package | 97°C/W |
| N package | 67°C/W |
| PW package | 128°C/W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT240 | | SN74AHCT240 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT240 | | SN74AHCT240 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 3 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT240 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5.4 | 7.4 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5.4 | 7.4 | 1 | 8.5 | |
| $t_{PZH}$* | OE | Y | $C_L$ = 15 pF | | 7.7 | 10.4 | 1 | 12 | ns |
| $t_{PZL}$* | | | | | 7.7 | 10.4 | 1 | 12 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 8.3 | 10.4 | 1 | 12 | ns |
| $t_{PLZ}$* | | | | | 8.3 | 10.4 | 1 | 12 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.9 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.9 | 8.4 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.2 | 11.4 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 8.2 | 11.4 | 1 | 13 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.8 | 11.4 | 1 | 13 | ns |
| $t_{PLZ}$ | | | | | 8.8 | 11.4 | 1 | 13 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT240 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5.4 | 7.4 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.4 | 7.4 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7.7 | 10.4 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.7 | 10.4 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 8.3 | 10.4 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 8.3 | 10.4 | 1 | 12 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.9 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.9 | 8.4 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.2 | 11.4 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 8.2 | 11.4 | 1 | 13 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.8 | 11.4 | 1 | 13 | ns |
| $t_{PLZ}$ | | | | | 8.8 | 11.4 | 1 | 13 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT240 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

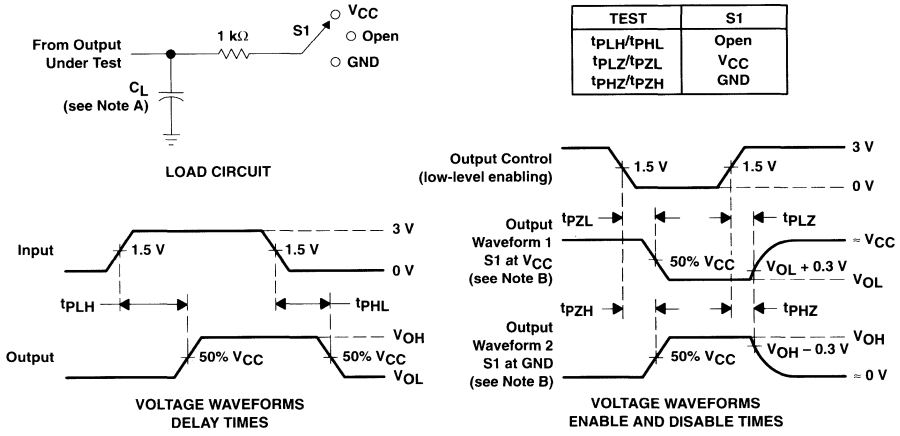
| PARAMETER | | SN74AHCT240 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.1 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 10 | pF |

## PARAMETER MEASUREMENT INFORMATION

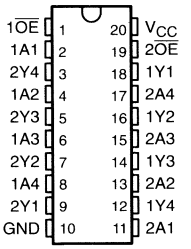



NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

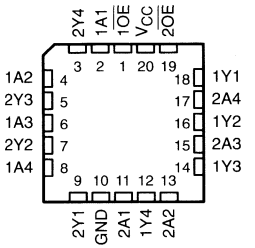
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC244 . . . J OR W PACKAGE**
**SN74AHC244 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC244 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'AHC244 are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

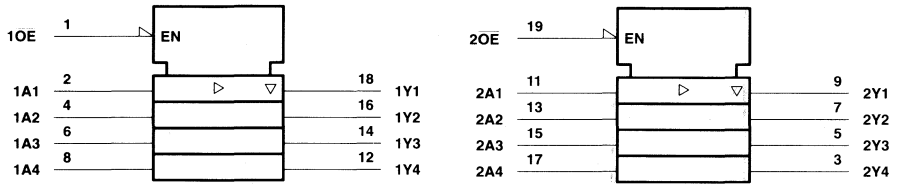
The SN54AHC244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC244 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

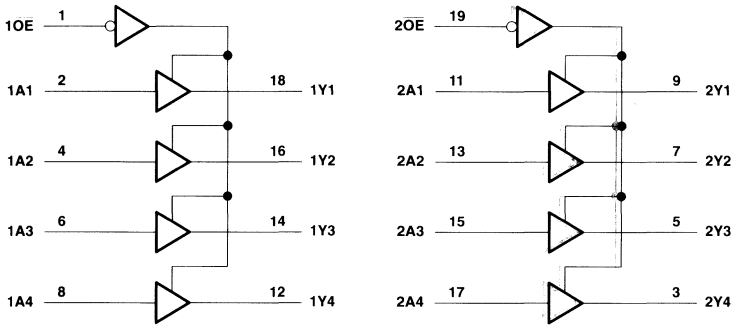
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DGV package ..... 146°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC244 | | SN74AHC244 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC244 | | SN74AHC244 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | Data inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| | Control inputs | | | | | ±0.1 | | ±1 | | ±1 | |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND, $V_I$ ($\overline{OE}$) = $V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| $C_o$ | | $V_O$ = $V_{CC}$ or GND | 5 V | | 3.5 | | | | | | pF |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC244 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5.8 | 8.4 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 5.8 | 8.4 | 1 | 10 | |
| $t_{PZH}$* | OE | Y | $C_L$ = 15 pF | | 6.6 | 10.6 | 1 | 12.5 | ns |
| $t_{PZL}$* | | | | | 6.6 | 10.6 | 1 | 12.5 | |
| $t_{PHZ}$* | OE | Y | $C_L$ = 15 pF | | 5 | 9.7 | 1 | 11 | ns |
| $t_{PLZ}$* | | | | | 5 | 9.7 | 1 | 11 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 8.3 | 11.9 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 8.3 | 11.9 | 1 | 13.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 9.1 | 14.1 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 9.1 | 14.1 | 1 | 16 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 10.3 | 14 | 1 | 16 | ns |
| $t_{PLZ}$ | | | | | 10.3 | 14 | 1 | 16 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC244 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5.8 | 8.4 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 5.8 | 8.4 | 1 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6.6 | 10.6 | 1 | 12.5 | ns |
| $t_{PZL}$ | | | | | 6.6 | 10.6 | 1 | 12.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 9.7 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 5 | 9.7 | 1 | 11 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 8.3 | 11.9 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 8.3 | 11.9 | 1 | 13.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 9.1 | 14.1 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 9.1 | 14.1 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 10.3 | 14 | 1 | 16 | ns |
| $t_{PLZ}$ | | | | | 10.3 | 14 | 1 | 16 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC244 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.9 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.9 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.7 | 7.3 | 1 | 8.5 | ns |
| $t_{PZL}$* | | | | | 4.7 | 7.3 | 1 | 8.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 7.2 | 1 | 8.5 | ns |
| $t_{PLZ}$* | | | | | 5 | 7.2 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.4 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.4 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 9.3 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 6.2 | 9.3 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.7 | 9.2 | 1 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 6.7 | 9.2 | 1 | 10.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC244 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.9 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.9 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.7 | 7.3 | 1 | 8.5 | ns |
| $t_{PZL}$ | | | | | 4.7 | 7.3 | 1 | 8.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 7.2 | 1 | 8.5 | ns |
| $t_{PLZ}$ | | | | | 5 | 7.2 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.4 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.4 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 9.3 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 6.2 | 9.3 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.7 | 9.2 | 1 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 6.7 | 9.2 | 1 | 10.5 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC244 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

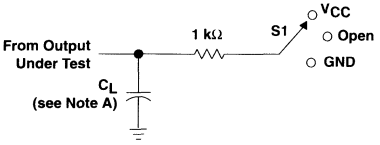
| PARAMETER | | SN74AHC244 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.5 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.2 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.8 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

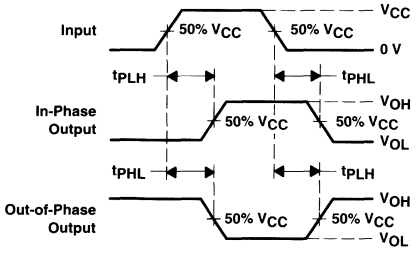
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 8.6 | pF |

## PARAMETER MEASUREMENT INFORMATION

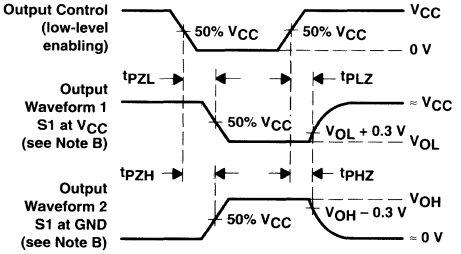



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



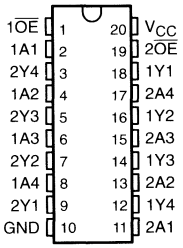

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

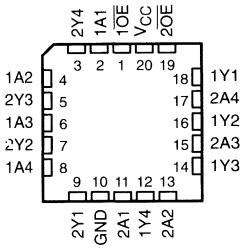
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

**SN54AHCT244 . . . J OR W PACKAGE**
**SN74AHCT244 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT244 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal buffers/drivers are designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'AHCT244 are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

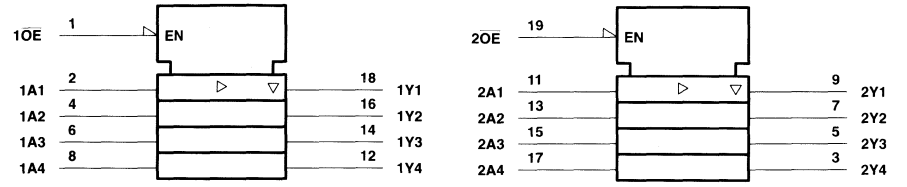
The SN54AHCT244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT244 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each buffer/driver)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

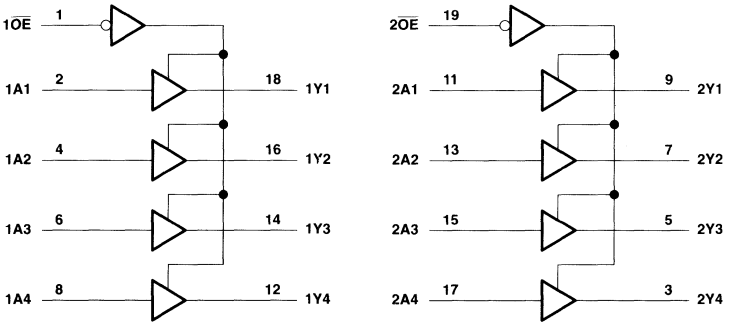
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DGV package ..... 146°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT244 | | SN74AHCT244 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT244 | | SN74AHCT244 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 3 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT244 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5.4 | 7.4 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5.4 | 7.4 | 1 | 8.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7.7 | 10.4 | 1 | 12 | ns |
| $t_{PZL}$* | | | | | 7.7 | 10.4 | 1 | 12 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 9.4 | 1 | 10 | ns |
| $t_{PLZ}$* | | | | | 5 | 9.4 | 1 | 10 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.9 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.9 | 8.4 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.2 | 11.4 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 8.2 | 11.4 | 1 | 13 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.8 | 11.4 | 1 | 13 | ns |
| $t_{PLZ}$ | | | | | 8.8 | 11.4 | 1 | 13 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT244 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5.4 | 7.4 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.4 | 7.4 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7.7 | 10.4 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.7 | 10.4 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 9.4 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 5 | 9.4 | 1 | 10 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.9 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.9 | 8.4 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.2 | 11.4 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 8.2 | 11.4 | 1 | 13 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.8 | 11.4 | 1 | 13 | ns |
| $t_{PLZ}$ | | | | | 8.8 | 11.4 | 1 | 13 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT244 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

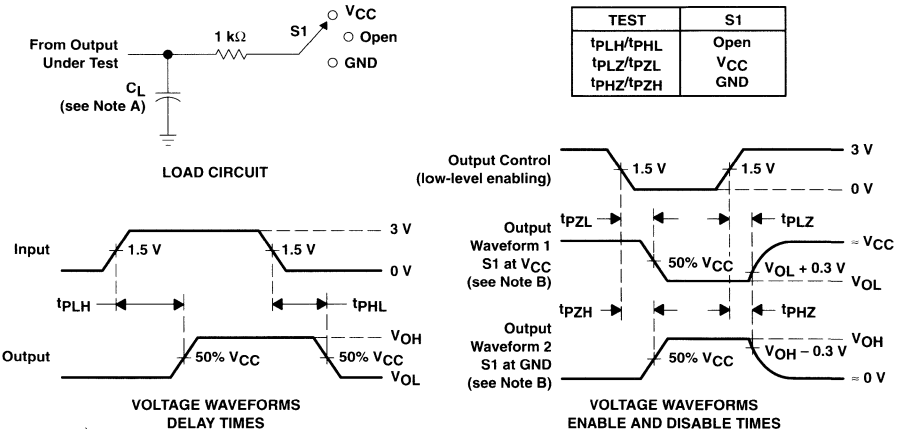
| PARAMETER | | SN74AHCT244 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.1 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 8.2 | pF |

## PARAMETER MEASUREMENT INFORMATION

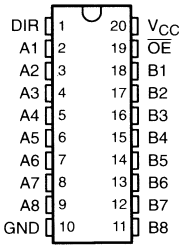



NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

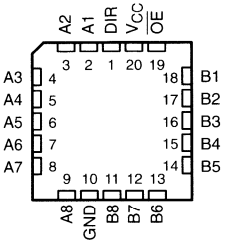
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC245 . . . J OR W PACKAGE**
**SN74AHC245 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC245 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHC245 octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

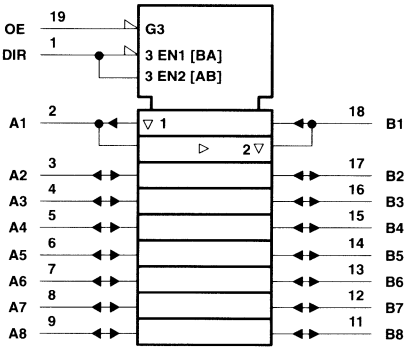
The SN54AHC245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC245 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

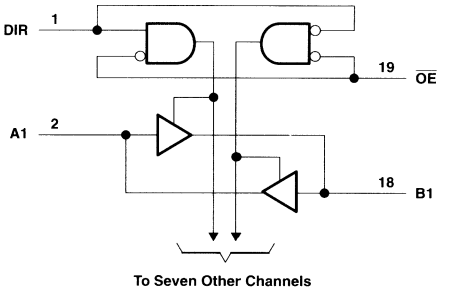
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DGV package ..... 146°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | | SN54AHC245 | | SN74AHC245 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | $\overline{OE}$ or DIR | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | A or B | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC245 | | SN74AHC245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | A or B inputs | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| | $\overline{OE}$ or DIR | | | | | ±0.1 | | ±1 | | ±1 | |
| $I_{OZ}$† | | $V_O = V_{CC}$ or GND, $V_I$ ($\overline{OE}$) = $V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $\overline{OE}$ or DIR | $V_I = V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_{io}$ | A or B inputs | $V_I = V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

† The parameter $I_{OZ}$ includes the input leakage current.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC245 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | B or A | $C_L$ = 15 pF | | 5.8 | 8.4 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 5.8 | 8.4 | 1 | 10 | |
| $t_{PZH}$* | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 8.5 | 13.2 | 1 | 15.5 | ns |
| $t_{PZL}$* | | | | | 8.5 | 13.2 | 1 | 15.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 8.9 | 12.5 | 1 | 15.5 | ns |
| $t_{PLZ}$* | | | | | 8.9 | 12.5 | 1 | 15.5 | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 50 pF | | 8.3 | 11.9 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 8.3 | 11.9 | 1 | 13.5 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 11 | 16.7 | 1 | 19 | ns |
| $t_{PZL}$ | | | | | 11 | 16.7 | 1 | 19 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 11.5 | 15.8 | 1 | 18 | ns |
| $t_{PLZ}$ | | | | | 11.5 | 15.8 | 1 | 18 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC245 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 15 pF | | 5.8 | 8.4 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 5.8 | 8.4 | 1 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 8.5 | 13.2 | 1 | 15.5 | ns |
| $t_{PZL}$ | | | | | 8.5 | 13.2 | 1 | 15.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 8.9 | 12.5 | 1 | 15.5 | ns |
| $t_{PLZ}$ | | | | | 8.9 | 12.5 | 1 | 15.5 | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 50 pF | | 8.3 | 11.9 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 8.3 | 11.9 | 1 | 13.5 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 11 | 16.7 | 1 | 19 | ns |
| $t_{PZL}$ | | | | | 11 | 16.7 | 1 | 19 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 11.5 | 15.8 | 1 | 18 | ns |
| $t_{PLZ}$ | | | | | 11.5 | 15.8 | 1 | 18 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC245 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | B or A | $C_L$ = 15 pF | | 4 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 4 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$* | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 5.8 | 8.5 | 1 | 10 | ns |
| $t_{PZL}$* | | | | | 5.8 | 8.5 | 1 | 10 | |
| $t_{PHZ}$* | OE | A or B | $C_L$ = 15 pF | | 5.6 | 7.8 | 1 | 9.2 | ns |
| $t_{PLZ}$* | | | | | 5.6 | 7.8 | 1 | 9.2 | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 50 pF | | 5.5 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | OE | A or B | $C_L$ = 50 pF | | 7.3 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.3 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 7 | 9.7 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 7 | 9.7 | 1 | 11 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC245 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 15 pF | | 4 | 5.5 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 4 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 5.8 | 8.5 | 1 | 10 | ns |
| $t_{PZL}$ | | | | | 5.8 | 8.5 | 1 | 10 | |
| $t_{PHZ}$ | OE | A or B | $C_L$ = 15 pF | | 5.6 | 7.8 | 1 | 9.2 | ns |
| $t_{PLZ}$ | | | | | 5.6 | 7.8 | 1 | 9.2 | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 50 pF | | 5.5 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.5 | 1 | 8.5 | |
| $t_{PZH}$ | OE | A or B | $C_L$ = 50 pF | | 7.3 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.3 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 7 | 9.7 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 7 | 9.7 | 1 | 11 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC245 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

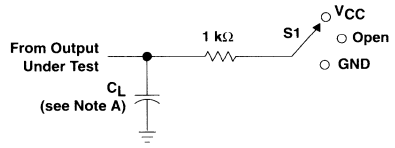
| PARAMETER | | SN74AHC245 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.9 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.9 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.3 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

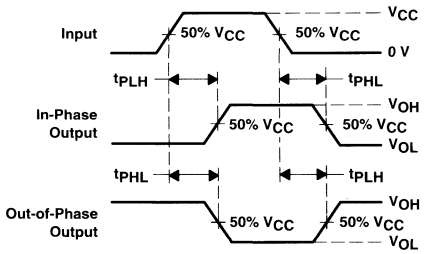
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 14 | pF |

## PARAMETER MEASUREMENT INFORMATION

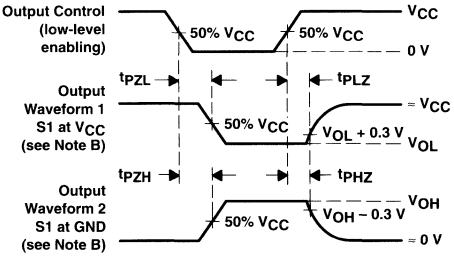



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



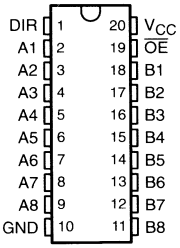

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

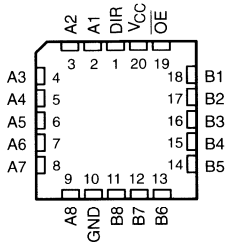
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

**SN54AHCT245 . . . J OR W PACKAGE**
**SN74AHCT245 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT245 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The 'AHCT245 allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

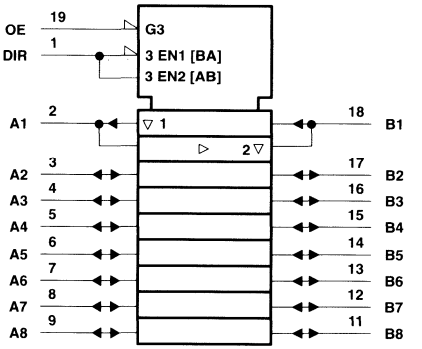
The SN54AHCT245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT245 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

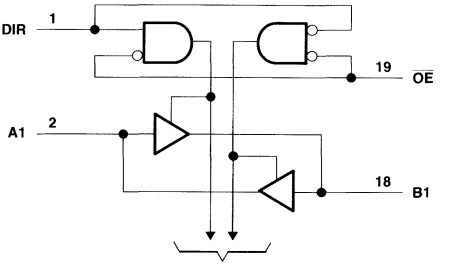
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DGV package ..... 146°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | SN54AHCT245 | | SN74AHCT245 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT245 | | SN74AHCT245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | A or B inputs† | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $\overline{OE}$ or DIR | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$‡ | | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $\overline{OE}$ or DIR | $V_I$ = $V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_{io}$ | A or B inputs | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

† For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT245 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | B or A | $C_L$ = 15 pF | | 4.5 | 7.7 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 4.5 | 7.7 | 1 | 10 | |
| $t_{PZH}$* | OE | A or B | $C_L$ = 15 pF | | 8.9 | 13.8 | 1 | 16 | ns |
| $t_{PZL}$* | | | | | 8.9 | 13.8 | 1 | 16 | |
| $t_{PHZ}$* | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 9.2 | 14.4 | 1 | 16.5 | ns |
| $t_{PLZ}$* | | | | | 9.2 | 14.4 | 1 | 16.5 | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 50 pF | | 5.3 | 8.7 | 1 | 11 | ns |
| $t_{PHL}$ | | | | | 5.3 | 8.7 | 1 | 11 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 9.7 | 14.8 | 1 | 17 | ns |
| $t_{PZL}$ | | | | | 9.7 | 14.8 | 1 | 17 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 10 | 15.4 | 1 | 17.5 | ns |
| $t_{PLZ}$ | | | | | 10 | 15.4 | 1 | 17.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT245 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 15 pF | | 4.5 | 7.7 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 4.5 | 7.7 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 8.9 | 13.8 | 1 | 15 | ns |
| $t_{PZL}$ | | | | | 8.9 | 13.8 | 1 | 15 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 9.2 | 14.4 | 1 | 15.5 | ns |
| $t_{PLZ}$ | | | | | 9.2 | 14.4 | 1 | 15.5 | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 50 pF | | 5.3 | 8.7 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 8.7 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 9.7 | 14.8 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 9.7 | 14.8 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 10 | 15.4 | 1 | 16.5 | ns |
| $t_{PLZ}$ | | | | | 10 | 15.4 | 1 | 16.5 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT245 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

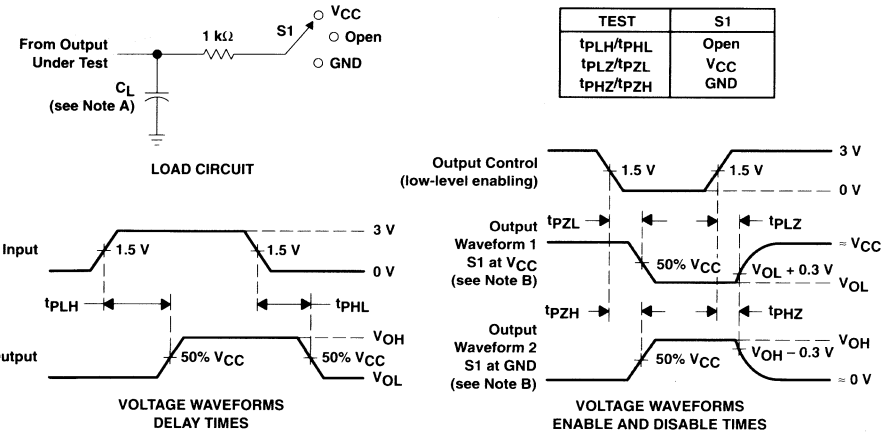
| PARAMETER | | SN74AHCT245 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 13 | pF |

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

# SN54AHC257, SN74AHC257
# QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SCLS349B – MAY 1996 – REVISED JUNE 1997

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

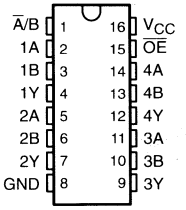
## description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 2-V to 5.5-V $V_{CC}$ operation.

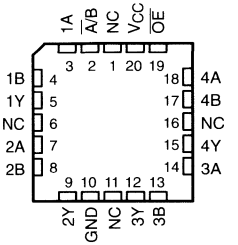
The 'AHC257 are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at a high logic level.

The SN54AHC257 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC257 is characterized for operation from –40°C to 85°C.

**SN54AHC257 . . . J OR W PACKAGE**
**SN74AHC257 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC257 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

**FUNCTION TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OE}$ | A/B | A | B | Y |
| H | X | X | X | Z |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.





TEXAS INSTRUMENTS
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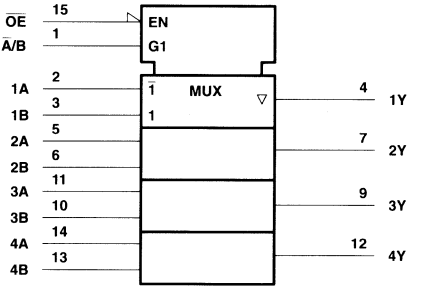
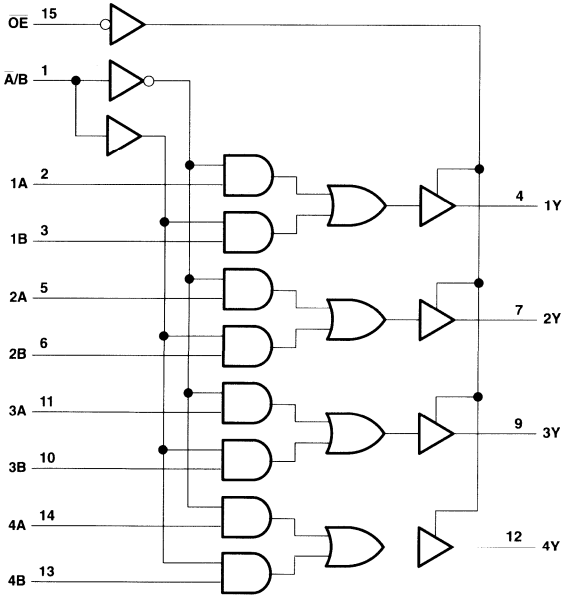
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.



## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC257 | | SN74AHC257 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC257 | | SN74AHC257 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC257 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 6.2 | 9.7 | 1 | 11.5 | ns |
| $t_{PHL}$* | | | | | 6.2 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$* | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 8.4 | 13.2 | 1 | 15.5 | ns |
| $t_{PHL}$* | | | | | 8.4 | 13.2 | 1 | 15.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PZL}$* | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$* | | | | | | | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.7 | 13.2 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.2 | 1 | 15 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 10.9 | 16.7 | 1 | 19 | ns |
| $t_{PHL}$ | | | | | 10.9 | 16.7 | 1 | 19 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PZL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC257 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 6.2 | 9.7 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.2 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 8.4 | 13.2 | 1 | 15.5 | ns |
| $t_{PHL}$ | | | | | 8.4 | 13.2 | 1 | 15.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.7 | 13.2 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.2 | 1 | 15 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 10.9 | 16.7 | 1 | 19 | ns |
| $t_{PHL}$ | | | | | 10.9 | 16.7 | 1 | 19 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PZL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC257 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$* | A/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PZL}$* | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$* | | | | | | | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | A/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC257 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$ | A/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PZL}$ | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | A/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |

PRODUCT PREVIEW

## noise characteristics $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

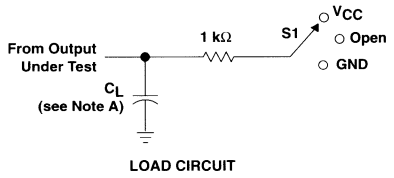
| PARAMETER | | SN74AHC257 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

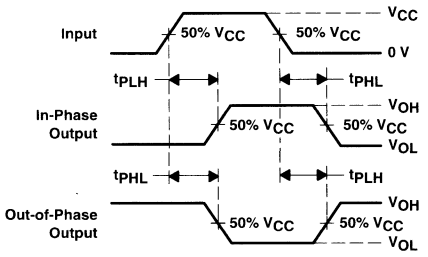
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 20 | pF |

## PARAMETER MEASUREMENT INFORMATION

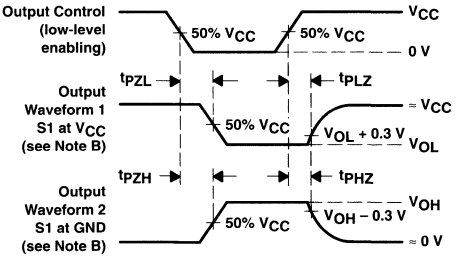



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

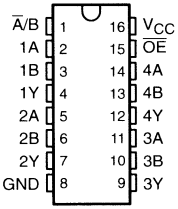
## description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V $V_{CC}$ operation.

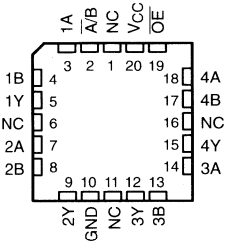
The 'AHCT257 are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at the high logic level.

The SN54AHCT257 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT257 is characterized for operation from –40°C to 85°C.

**SN54AHCT257 . . . J OR W PACKAGE**
**SN74AHCT257 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT257 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

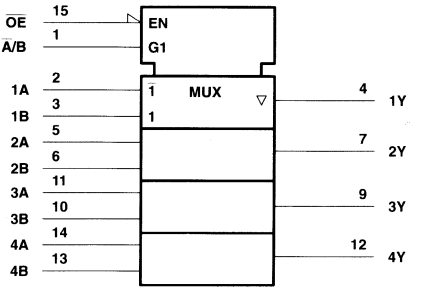
**FUNCTION TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OE}$ | A/B | A | B | Y |
| H | X | X | X | Z |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

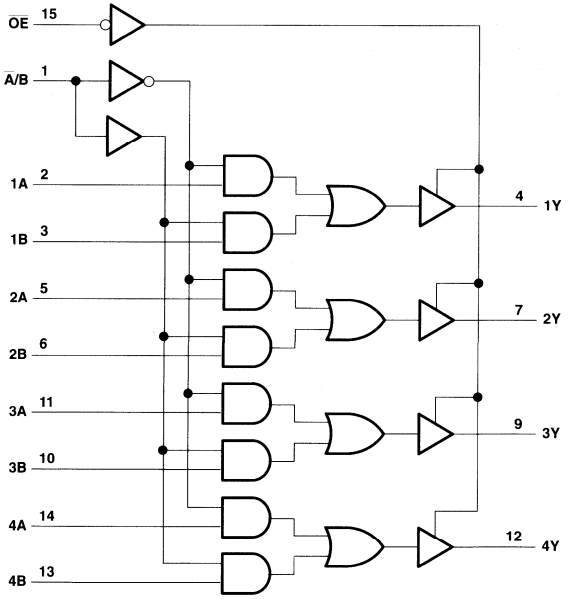
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | SN54AHCT257 | | SN74AHCT257 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall time | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT257 | | SN74AHCT257 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT257 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$* | A/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PZH}$* | OE | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PZL}$* | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$* | | | | | | | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PLH}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT257 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PZL}$ | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PLH}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |

## noise characteristics $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

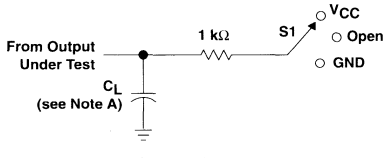
| PARAMETER | | SN74AHCT257 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

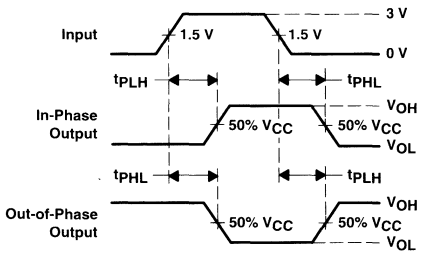
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 20 | pF |

## PARAMETER MEASUREMENT INFORMATION

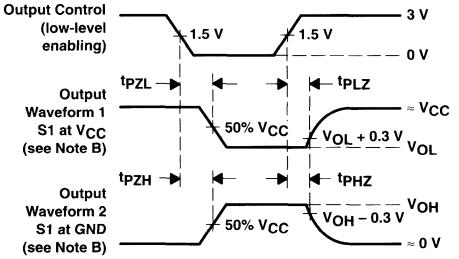



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

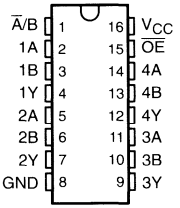
## description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 2-V to 5.5-V $V_{CC}$ operation.

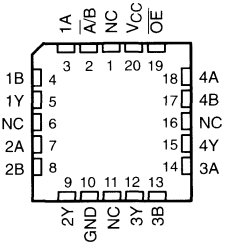
The 'AHC258 are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at a high logic level.

The SN54AHC258 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC258 is characterized for operation from –40°C to 85°C.

**SN54AHC258 . . . J OR W PACKAGE**
**SN74AHC258 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC258 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

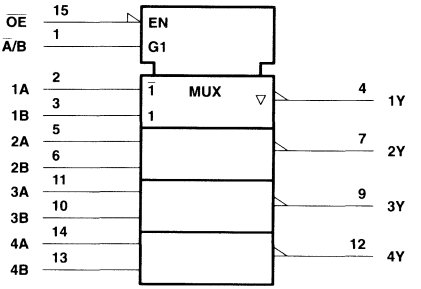
**FUNCTION TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OE}$ | $\overline{A}$/B | A | B | Y |
| H | X | X | X | Z |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

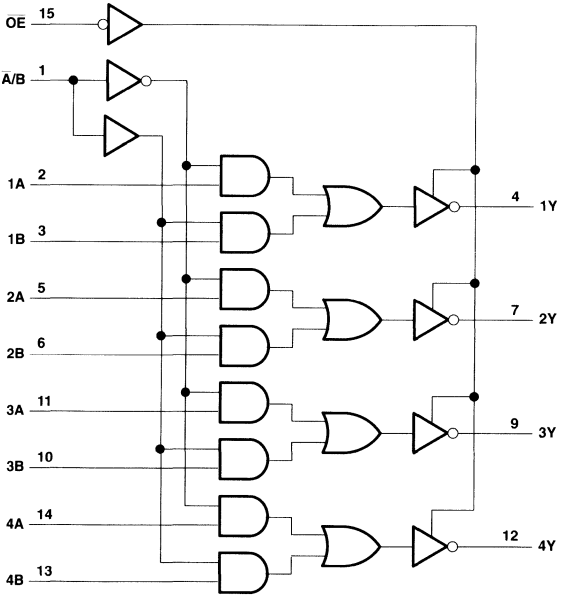
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.



## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
N package . . . . . 78°C/W
PW package . . . . . 149°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | | SN54AHC258 | | SN74AHC258 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC258 | | SN74AHC258 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC258 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 6.2 | 9.7 | 1 | 11.5 | ns |
| $t_{PHL}$* | | | | | 6.2 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$* | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 8.4 | 13.2 | 1 | 15.5 | ns |
| $t_{PHL}$* | | | | | 8.4 | 13.2 | 1 | 15.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PZL}$* | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$* | | | | | | | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.7 | 13.2 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.2 | 1 | 15 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 10.9 | 16.7 | 1 | 19 | ns |
| $t_{PHL}$ | | | | | 10.9 | 16.7 | 1 | 19 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PZL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC258 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 6.2 | 9.7 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.2 | 9.7 | 1 | 11.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 8.4 | 13.2 | 1 | 15.5 | ns |
| $t_{PHL}$ | | | | | 8.4 | 13.2 | 1 | 15.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8.7 | 13.2 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.2 | 1 | 15 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 10.9 | 16.7 | 1 | 19 | ns |
| $t_{PHL}$ | | | | | 10.9 | 16.7 | 1 | 19 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PZL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC258 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$* | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PZL}$* | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PHZ}$* | OE | Y | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$* | | | | | | | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC258 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PZL}$ | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |

## noise characteristics $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

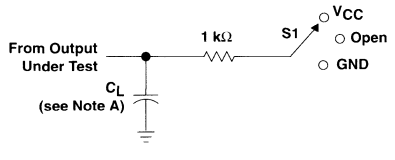
| PARAMETER | | SN74AHC258 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

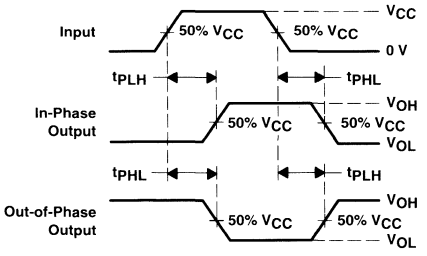
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 20 | pF |

## PARAMETER MEASUREMENT INFORMATION

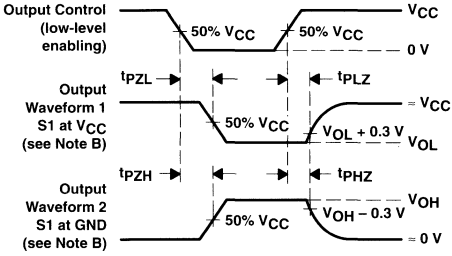



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

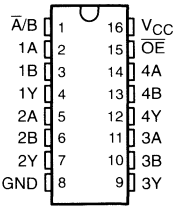
## description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V $V_{CC}$ operation.

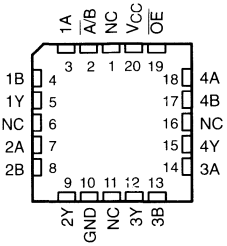
The 'AHCT258 are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at the high logic level.

The SN54AHCT258 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT258 is characterized for operation from –40°C to 85°C.

**SN54AHCT258 . . . J OR W PACKAGE**
**SN74AHCT258 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT258 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

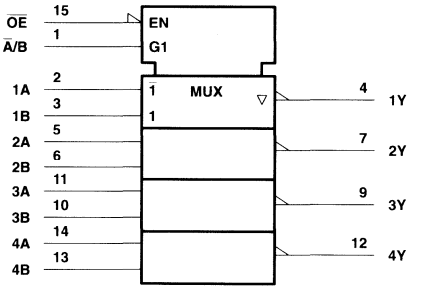
**FUNCTION TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OE}$ | A/B | A | B | Y |
| H | X | X | X | Z |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

PRODUCT PREVIEW

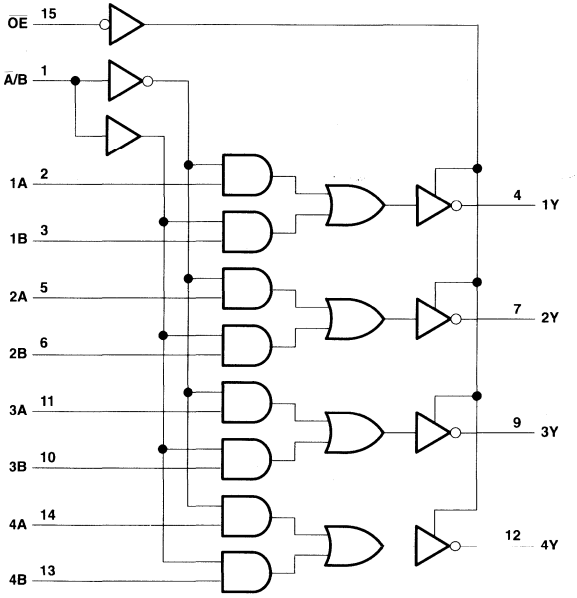
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | SN54AHCT258 | | SN74AHCT258 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall time | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT258 | | SN74AHCT258 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT258 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$* | A/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PZH}$* | OE | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PZL}$* | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PHZ}$* | OE | Y | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$* | | | | | | | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | A/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PLH}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT258 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 4.1 | 6.4 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 4.1 | 6.4 | 1 | 7.5 | |
| $t_{PLH}$ | A/B | Y | $C_L$ = 15 pF | | 5.3 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 8.1 | 1 | 9.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PZL}$ | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.6 | 8.4 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.4 | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{A}$/B | Y | $C_L$ = 50 pF | | 6.8 | 10.1 | 1 | 11.5 | ns |
| $t_{PLH}$ | | | | | 6.8 | 10.1 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |

PRODUCT PREVIEW

## noise characteristics $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

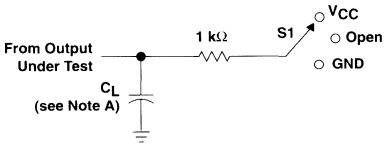
| PARAMETER | | SN74AHCT258 MIN | SN74AHCT258 MAX | UNIT |
|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

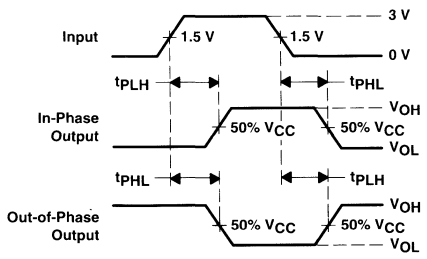
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 20 | pF |

## PARAMETER MEASUREMENT INFORMATION

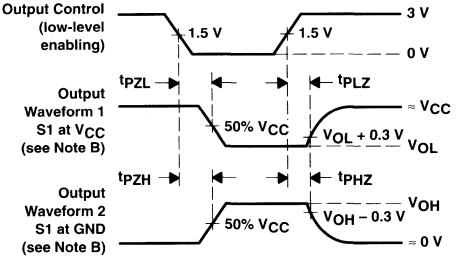



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

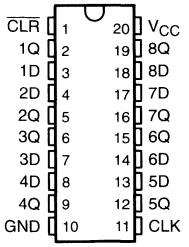
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

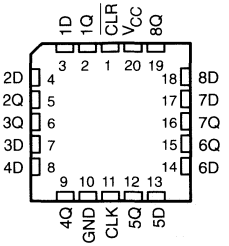
PRODUCT PREVIEW

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Contain Eight Flip-Flops With Single-Rail Outputs**
- **Direct Clear Input**
- **Individual Data Input to Each Flip-Flop**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC273 . . . J OR W PACKAGE**
**SN74AHC273 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC273 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{CLR}$) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

The SN54AHC273 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC273 is characterized for operation from –40°C to 85 °C.

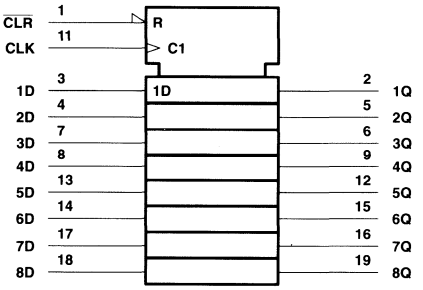
**FUNCTION TABLE**
**(each flip-flop)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{CLR}$ | CLK | D | Q |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | $Q_0$ |

PRODUCT PREVIEW

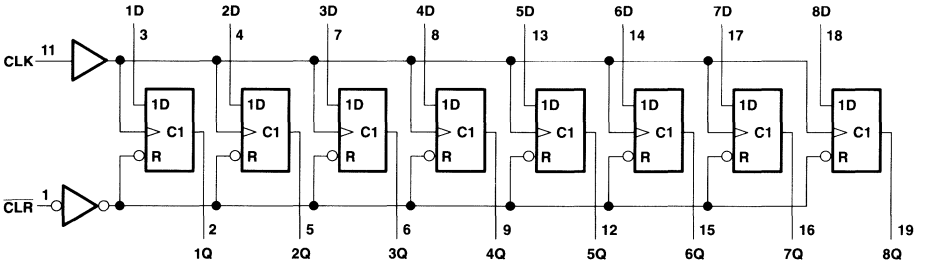
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†

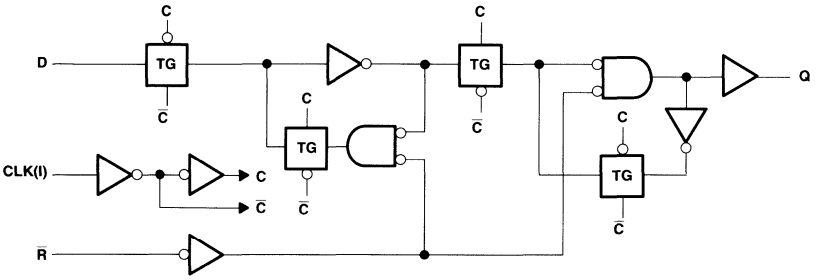



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## logic diagram, each flip-flop (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DGV package ..... 146°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 5 | | 6 | | 6 | | ns |
| | | CLK high or low | 5 | | 6.5 | | 6.5 | | |
| $t_{su}$ | Setup time | Data before CLK↑ | 5.5 | | 6.5 | | 6.5 | | ns |
| | | $\overline{CLR}$ before CLK↑ | 2.5 | | 2.5 | | 2.5 | | |
| $t_h$ | Hold time, data after CLK↑ | | 1 | | 1 | | 1 | | ns |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 5 | | 5 | | 5 | | ns |
| | | CLK high or low | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time | Data before CLK↑ | 4.5 | | 4.5 | | 4.5 | | ns |
| | | $\overline{CLR}$ before CLK↑ | 2 | | 2 | | 2 | | |
| $t_h$ | Hold time, data after CLK↑ | | 1 | | 1 | | 1 | | ns |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC273 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 75 | 120 | | 65 | | MHz |
| | | | $C_L$ = 50 pF | 50 | 75 | | 45 | | |
| $t_{PHL}$* | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 8.9 | 13.6 | 1 | 16 | ns |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PHL}$* | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 11.4 | 17.1 | 1 | 19.5 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC273 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 75 | 120 | | 65 | | MHz |
| | | | $C_L$ = 50 pF | 50 | 75 | | 45 | | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 8.9 | 13.6 | 1 | 16 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 8.7 | 13.6 | 1 | 16 | ns |
| $t_{PHL}$ | | | | | 8.7 | 13.6 | 1 | 16 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 11.4 | 17.1 | 1 | 19.5 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC273 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 120 | 165 | | 100 | | MHz |
| | | | $C_L$ = 50 pF | 80 | 110 | | 70 | | |
| $t_{PHL}$* | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 5.2 | 8.5 | 1 | 10 | ns |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 5.8 | 9 | 1 | 10.5 | ns |
| $t_{PHL}$* | | | | | 5.8 | 9 | 1 | 10.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 6.7 | 10.5 | 1 | 12 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 7.3 | 11 | 1 | 12.5 | ns |
| $t_{PHL}$ | | | | | 7.3 | 11 | 1 | 12.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC273 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 120 | 165 | | 100 | | MHz |
| | | | $C_L$ = 50 pF | 80 | 110 | | 70 | | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 5.2 | 8.5 | 1 | 10 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 5.8 | 9 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5.8 | 9 | 1 | 10.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 6.7 | 10.5 | 1 | 12 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 7.3 | 11 | 1 | 12.5 | ns |
| $t_{PHL}$ | | | | | 7.3 | 11 | 1 | 12.5 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC273 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

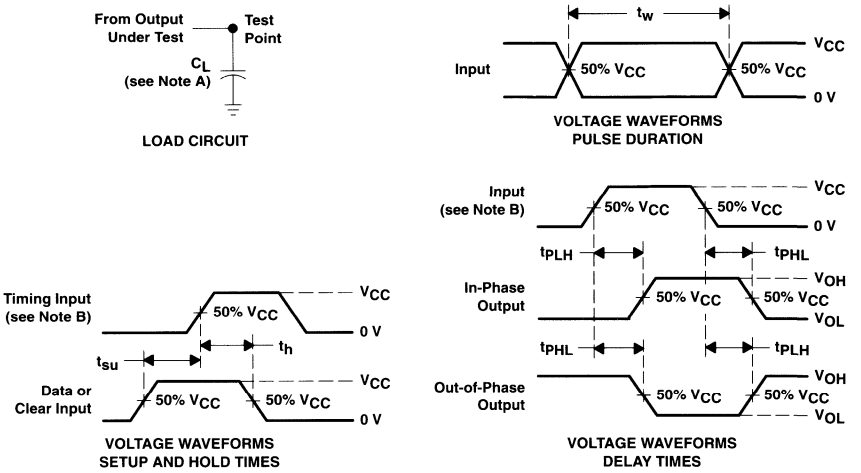
| PARAMETER | | SN74AHC273 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per flip-flop | No load | 31 | pF |

## PARAMETER MEASUREMENT INFORMATION



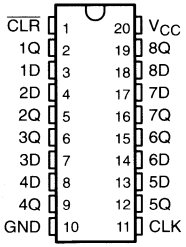

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

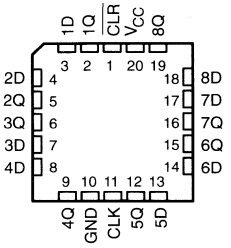
PRODUCT PREVIEW

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Contain Eight Flip-Flops With Single-Rail Outputs**
- **Direct Clear Input**
- **Individual Data Input to Each Flip-Flop**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT273 . . . J OR W PACKAGE**
**SN74AHCT273 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT273 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{CLR}$) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

The SN54AHCT273 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT273 is characterized for operation from –40°C to 85 °C.

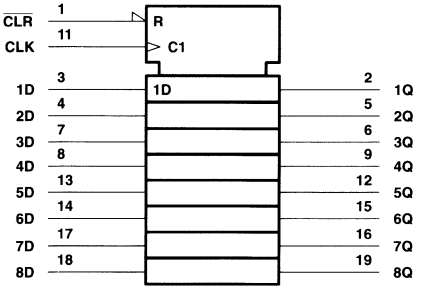
**FUNCTION TABLE**
**(each flip-flop)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{CLR}$ | CLK | D | Q |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | $Q_0$ |

PRODUCT PREVIEW

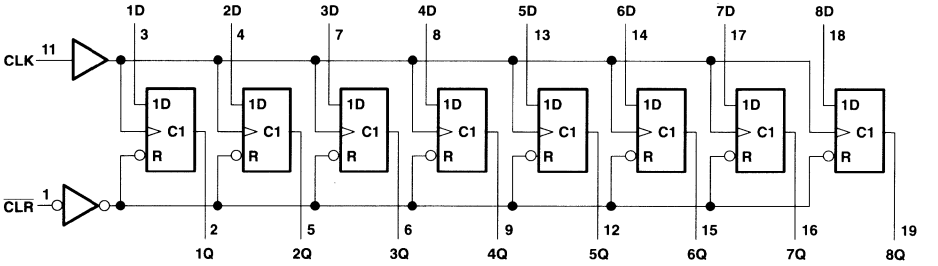
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†

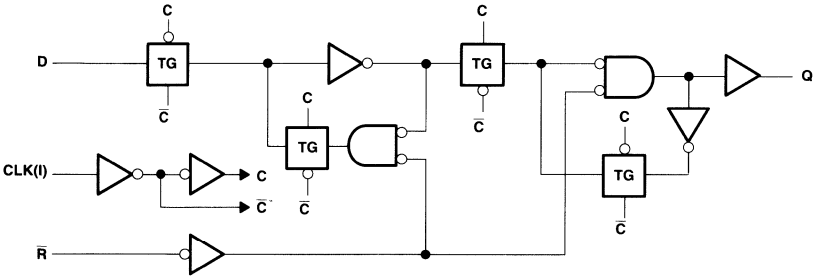



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## logic diagram, each flip-flop (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 115°C/W
DGV package . . . . . 146°C/W
DW package . . . . . 97°C/W
N package . . . . . 67°C/W
PW package . . . . . 128°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT273 | | SN74AHCT273 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall time | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT273 | | SN74AHCT273 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4.5 | 10 | | | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHCT273 | | SN74AHCT273 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 5 | | 5 | | 5 | | ns |
| | | CLK high or low | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time | Data before CLK↑ | 4.5 | | 4.5 | | 4.5 | | ns |
| | | $\overline{CLR}$ before CLK↑ | 2 | | 2 | | 2 | | |
| $t_h$ | Hold time, data after CLK↑ | | 1 | | 1 | | 1 | | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT273 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 120 | 165 | | 100 | | MHz |
| | | | $C_L$ = 50 pF | 80 | 110 | | 70 | | |
| $t_{PHL}$* | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 5.2 | 8.5 | 1 | 10 | ns |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 5.8 | 9 | 1 | 10.5 | ns |
| $t_{PHL}$* | | | | | 5.8 | 9 | 1 | 10.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 6.7 | 10.5 | 1 | 12 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 7.3 | 11 | 1 | 12.5 | ns |
| $t_{PHL}$ | | | | | 7.3 | 11 | 1 | 12.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT273 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 120 | 165 | | 100 | | MHz |
| | | | $C_L$ = 50 pF | 80 | 110 | | 70 | | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 5.2 | 8.5 | 1 | 10 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 5.8 | 9 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5.8 | 9 | 1 | 10.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 6.7 | 10.5 | 1 | 12 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 7.3 | 11 | 1 | 12.5 | ns |
| $t_{PHL}$ | | | | | 7.3 | 11 | 1 | 12.5 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT273 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

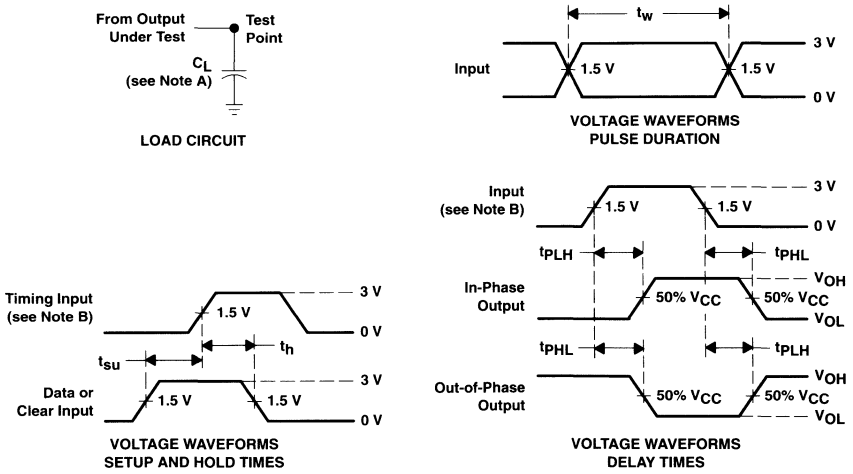
| PARAMETER | | SN74AHCT273 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per flip-flop | No load | 31 | pF |

## PARAMETER MEASUREMENT INFORMATION



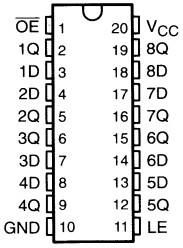

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

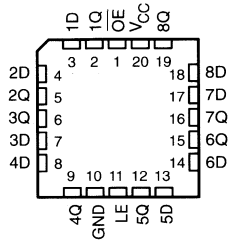
PRODUCT PREVIEW

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC373 . . . J OR W PACKAGE**
**SN74AHC373 . . . DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC373 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHC373 are octal transparent D-type latches.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

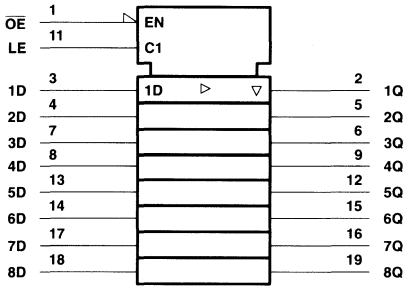
The SN54AHC373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC373 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

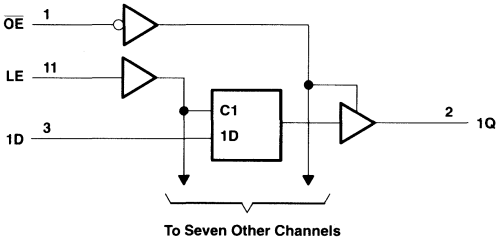
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC373 | | SN74AHC373 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC373 | | SN74AHC373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{OZ}$ | $V_I$ = $V_{IH}$ or $V_{IL}$, $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 6 | | | | | | pF |

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| | | $T_A$ = 25°C | | SN54AHC373 | | SN74AHC373 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 4 | | 4 | | 4 | | ns |
| $t_h$ | Hold time, data after LE↓ | 1 | | 1 | | 1 | | ns |

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| | | $T_A$ = 25°C | | SN54AHC373 | | SN74AHC373 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 4 | | 4 | | 4 | | ns |
| $t_h$ | Hold time, data after LE↓ | 1 | | 1 | | 1 | | ns |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC373 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | D | Q | $C_L$ = 15 pF | | 7.3 | 11.4 | 1 | 13.5 | ns |
| $t_{PHL}$* | | | | | 7.3 | 11.4 | 1 | 13.5 | |
| $t_{PLH}$* | LE | Q | $C_L$ = 15 pF | | 7 | 11 | 1 | 13 | ns |
| $t_{PHL}$* | | | | | 7 | 11 | 1 | 13 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.3 | 11.4 | 1 | 13.5 | ns |
| $t_{PZL}$* | | | | | 7.3 | 11.4 | 1 | 13.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7 | 10 | 1 | 12 | ns |
| $t_{PLZ}$* | | | | | 7 | 10 | 1 | 12 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 9.8 | 14.9 | 1 | 17 | ns |
| $t_{PHL}$ | | | | | 9.8 | 14.9 | 1 | 17 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 9.5 | 14.5 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | | 9.5 | 14.5 | 1 | 16.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.8 | 14.9 | 1 | 17 | ns |
| $t_{PZL}$ | | | | | 9.8 | 14.9 | 1 | 17 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.5 | 13.2 | 1 | 15 | ns |
| $t_{PLZ}$ | | | | | 9.5 | 13.2 | 1 | 15 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC373 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | D | Q | $C_L$ = 15 pF | | 7.3 | 11.4 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 7.3 | 11.4 | 1 | 13.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 15 pF | | 7 | 11 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 7 | 11 | 1 | 13 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.3 | 11.4 | 1 | 13.5 | ns |
| $t_{PZL}$ | | | | | 7.3 | 11.4 | 1 | 13.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7 | 10 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 7 | 10 | 1 | 12 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 9.8 | 14.9 | 1 | 17 | ns |
| $t_{PHL}$ | | | | | 9.8 | 14.9 | 1 | 17 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 9.5 | 14.5 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | | 9.5 | 14.5 | 1 | 16.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.8 | 14.9 | 1 | 17 | ns |
| $t_{PZL}$ | | | | | 9.8 | 14.9 | 1 | 17 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.5 | 13.2 | 1 | 15 | ns |
| $t_{PLZ}$ | | | | | 9.5 | 13.2 | 1 | 15 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC373 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | D | Q | $C_L$ = 15 pF | | 5 | 7.2 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5 | 7.2 | 1 | 8.5 | |
| $t_{PLH}$* | LE | Q | $C_L$ = 15 pF | | 4.9 | 7.2 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 7.2 | 1 | 8.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.5 | 8.1 | 1 | 9.5 | ns |
| $t_{PZL}$* | | | | | 5.5 | 8.1 | 1 | 9.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5 | 7.2 | 1 | 8.5 | ns |
| $t_{PLZ}$* | | | | | 5 | 7.2 | 1 | 8.5 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 6.5 | 9.2 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.5 | 9.2 | 1 | 10.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 6.4 | 9.2 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 9.2 | 1 | 10.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7 | 10.1 | 1 | 11.5 | ns |
| $t_{PZL}$ | | | | | 7 | 10.1 | 1 | 11.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.5 | 9.2 | 1 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 6.5 | 9.2 | 1 | 10.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC373 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | D | Q | $C_L$ = 15 pF | | 5 | 7.2 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5 | 7.2 | 1 | 8.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 15 pF | | 4.9 | 7.2 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 4.9 | 7.2 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.5 | 8.1 | 1 | 9.5 | ns |
| $t_{PZL}$ | | | | | 5.5 | 8.1 | 1 | 9.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5 | 7.2 | 1 | 8.5 | ns |
| $t_{PLZ}$ | | | | | 5 | 7.2 | 1 | 8.5 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 6.5 | 9.2 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.5 | 9.2 | 1 | 10.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 6.4 | 9.2 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 9.2 | 1 | 10.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7 | 10.1 | 1 | 11.5 | ns |
| $t_{PZL}$ | | | | | 7 | 10.1 | 1 | 11.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.5 | 9.2 | 1 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 6.5 | 9.2 | 1 | 10.5 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC373 | | UNIT |
|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | MIN MAX | |
| | | | MIN | MAX | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | 1.5 | 1.5 | ns |
| | | 5 V ± 0.5 V | 1 | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

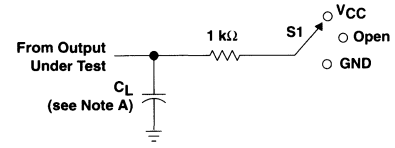
| PARAMETER | | SN74AHC373 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.1 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

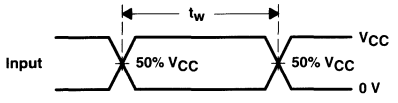
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 18 | pF |

## PARAMETER MEASUREMENT INFORMATION

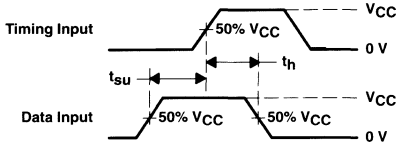



LOAD CIRCUIT

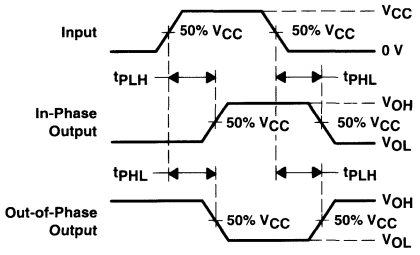
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



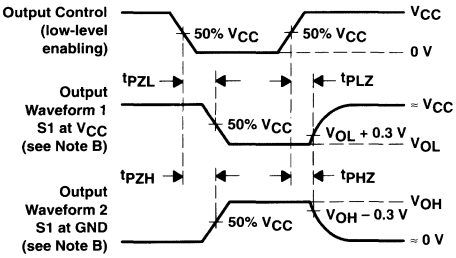

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES



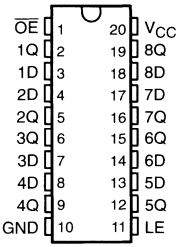

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

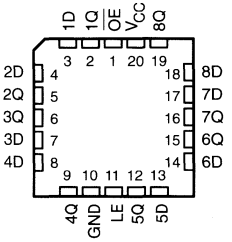
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT373 . . . J OR W PACKAGE**
**SN74AHCT373 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT373 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHCT373 are octal-transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

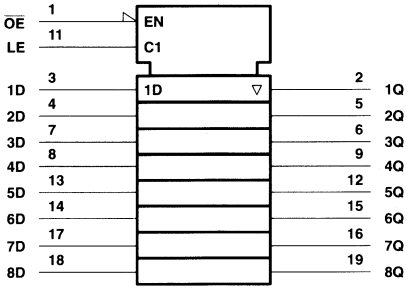
The SN54AHCT373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT373 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

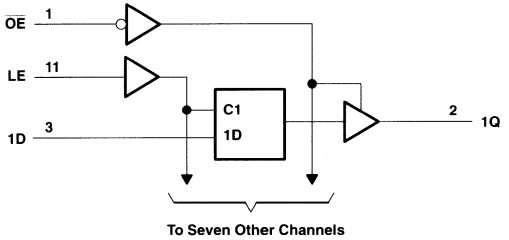
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DGV package ..... 146°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT373 | | SN74AHCT373 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT373 | | SN74AHCT373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 9 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHCT373 | | SN74AHCT373 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, $\overline{LE}$ high | 6.5 | | 6.5 | | 6.5 | | ns |
| $t_{su}$ | Setup time, data before $\overline{LE}\downarrow$ | 1.5 | | 1.5 | | 1.5 | | ns |
| $t_h$ | Hold time, data after $\overline{LE}\downarrow$ | 3.5 | | 3.5 | | 3.5 | | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT373 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | D | Q | $C_L$ = 15 pF | | 5.1 | 8.5 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.1 | 8.5 | 1 | 9.5 | |
| $t_{PLH}$* | LE | Q | $C_L$ = 15 pF | | 7.7 | 12.3 | 1 | 13.5 | ns |
| $t_{PHL}$* | | | | | 7.7 | 12.3 | 1 | 13.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 6.3 | 10.9 | 1 | 12.5 | ns |
| $t_{PZL}$* | | | | | 6.3 | 10.9 | 1 | 12.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 6 | 10.2 | 1 | 11 | ns |
| $t_{PLZ}$* | | | | | 6 | 10.2 | 1 | 11 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 5.9 | 9.5 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5.9 | 9.5 | 1 | 10.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 8.5 | 13.3 | 1 | 14.5 | ns |
| $t_{PHL}$ | | | | | 8.5 | 13.3 | 1 | 14.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7.1 | 11.9 | 1 | 13.5 | ns |
| $t_{PZL}$ | | | | | 7.1 | 11.9 | 1 | 13.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.8 | 11.2 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 6.8 | 11.2 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT373 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | D | Q | $C_L$ = 15 pF | | 5.1 | 8.5 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.1 | 8.5 | 1 | 9.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 15 pF | | 7.7 | 12.3 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 7.7 | 12.3 | 1 | 13.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 6.3 | 10.9 | 1 | 12.5 | ns |
| $t_{PZL}$ | | | | | 6.3 | 10.9 | 1 | 12.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 6 | 10.2 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 6 | 10.2 | 1 | 11 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 5.9 | 9.5 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5.9 | 9.5 | 1 | 10.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 8.5 | 13.3 | 1 | 14.5 | ns |
| $t_{PHL}$ | | | | | 8.5 | 13.3 | 1 | 14.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7.1 | 11.9 | 1 | 13.5 | ns |
| $t_{PZL}$ | | | | | 7.1 | 11.9 | 1 | 13.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.8 | 11.2 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 6.8 | 11.2 | 1 | 12 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT373 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

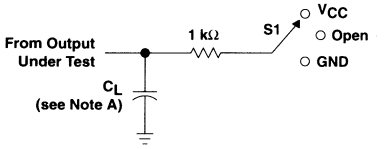
| PARAMETER | | SN74AHCT373 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | 1.2 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | –1.2 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.1 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

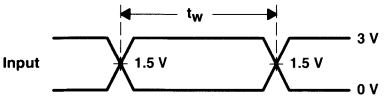
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 17 | pF |

## PARAMETER MEASUREMENT INFORMATION

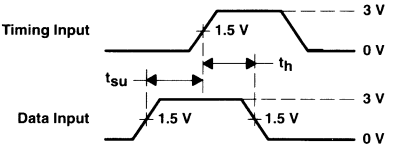



LOAD CIRCUIT

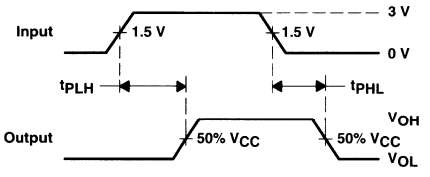
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



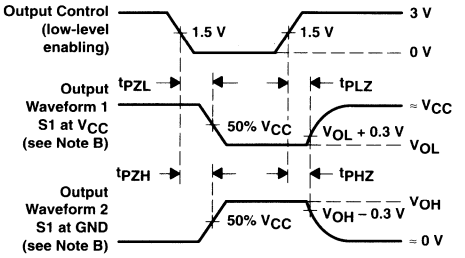

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES



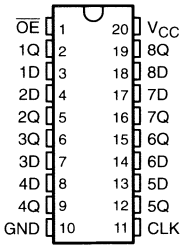

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

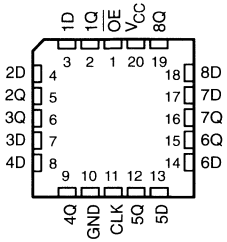
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- **3-State Outputs Drive Bus Lines Directly**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC374 . . . J OR W PACKAGE**
**SN74AHC374 . . . DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC374 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHC374 are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

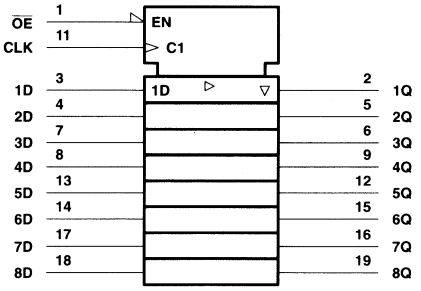
The SN54AHC374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC374 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each flip-flop)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

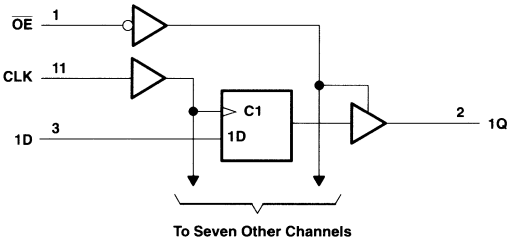
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I < 0$) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC374 | | SN74AHC374 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC374 | | SN74AHC374 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 6 | | | | | | pF |

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| | | $T_A$ = 25°C | | SN54AHC374 | | SN74AHC374 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 5 | | 5.5 | | 5.5 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 4.5 | | 4 | | 4 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 2 | | 2 | | 2 | | ns |

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| | | $T_A$ = 25°C | | SN54AHC374 | | SN74AHC374 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 3 | | 3 | | 3 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 2 | | 2 | | 2 | | ns |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC374 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 80 | 130 | | 70 | | MHz |
| | | | $C_L$ = 50 pF | 55 | 85 | | 50 | | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 8.1 | 12.7 | 1 | 15 | ns |
| $t_{PHL}$* | | | | | 8.1 | 12.7 | 1 | 15 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.1 | 11 | 1 | 13 | ns |
| $t_{PZL}$* | | | | | 7.1 | 11 | 1 | 13 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.5 | 10.5 | 1 | 12.5 | ns |
| $t_{PLZ}$* | | | | | 7.5 | 10.5 | 1 | 12.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 10.6 | 16.2 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.6 | 16.2 | 1 | 18.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.6 | 14.5 | 1 | 16.5 | ns |
| $t_{PZL}$ | | | | | 9.6 | 14.5 | 1 | 16.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 10.2 | 14 | 1 | 16 | ns |
| $t_{PLZ}$ | | | | | 10.2 | 14 | 1 | 16 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC374 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 80 | 130 | | 70 | | MHz |
| | | | $C_L$ = 50 pF | 55 | 85 | | 50 | | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 8.1 | 12.7 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.1 | 12.7 | 1 | 15 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.1 | 11 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 7.1 | 11 | 1 | 13 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.5 | 10.5 | 1 | 12.5 | ns |
| $t_{PLZ}$ | | | | | 7.5 | 10.5 | 1 | 12.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 10.6 | 16.2 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.6 | 16.2 | 1 | 18.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.6 | 14.5 | 1 | 16.5 | ns |
| $t_{PZL}$ | | | | | 9.6 | 14.5 | 1 | 16.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 10.2 | 14 | 1 | 16 | ns |
| $t_{PLZ}$ | | | | | 10.2 | 14 | 1 | 16 | |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC374 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 130 | 185 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 120 | | 75 | | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 5.4 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.4 | 8.1 | 1 | 9.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.1 | 7.6 | 1 | 9 | ns |
| $t_{PZL}$* | | | | | 5.1 | 7.6 | 1 | 9 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$* | | | | | 4.6 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.9 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.9 | 10.1 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.6 | 9.6 | 1 | 11 | ns |
| $t_{PZL}$ | | | | | 6.6 | 9.6 | 1 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC374 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 130 | 185 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 120 | | 75 | | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 5.4 | 8.1 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.4 | 8.1 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.1 | 7.6 | 1 | 9 | ns |
| $t_{PZL}$ | | | | | 5.1 | 7.6 | 1 | 9 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$ | | | | | 4.6 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.9 | 10.1 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.9 | 10.1 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.6 | 9.6 | 1 | 11 | ns |
| $t_{PZL}$ | | | | | 6.6 | 9.6 | 1 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC374 | | UNIT |
|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | MIN MAX | |
| | | | MIN MAX | | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | 1.5 | 1.5 | ns |
| | | 5 V ± 0.5 V | 1 | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

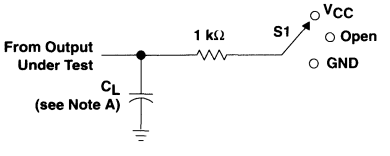
| PARAMETER | | SN74AHC374 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.5 | 1 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.5 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

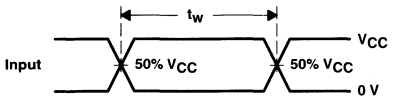
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 32 | pF |

## PARAMETER MEASUREMENT INFORMATION

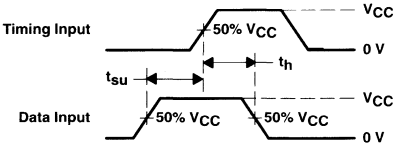



LOAD CIRCUIT

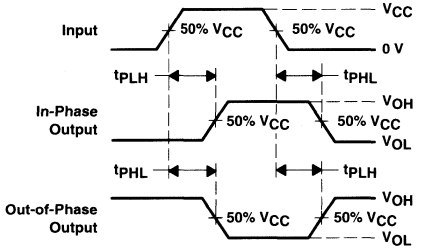
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



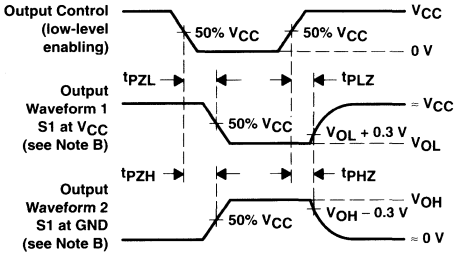

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES



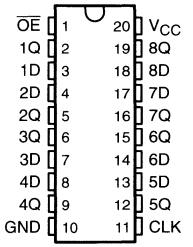

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

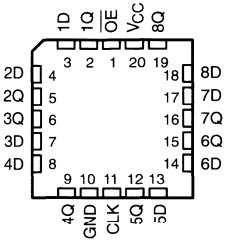
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT374 . . . J OR W PACKAGE**
**SN74AHCT374 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT374 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHCT374 are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

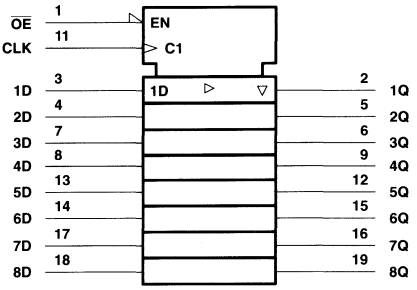
The SN54AHCT374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT374 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each flip-flop)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

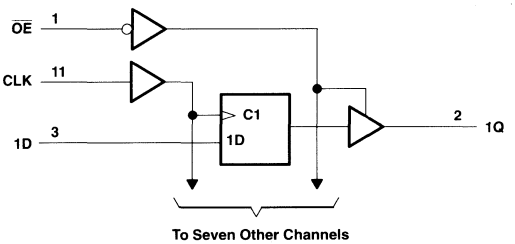
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DGV package ..... 146°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT374 | | SN74AHCT374 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT374 | | SN74AHCT374 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND, $V_I = V_{IH}$ or $V_{IL}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 9 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHCT374 | | SN74AHCT374 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 6.5 | | 6.5 | | 6.5 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 2.5 | | 2.5 | | 2.5 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 2.5 | | 2.5 | | 2.5 | | ns |

### switching characteristics over recommended free-air temperature operating range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT374 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 90 | 140 | | 80 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 130 | | 75 | | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 5.6 | 9.4 | 1 | 10.5 | ns |
| $t_{PHL}$* | | | | | 5.6 | 9.4 | 1 | 10.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 6.5 | 10.2 | 1 | 11.5 | ns |
| $t_{PZL}$* | | | | | 6.5 | 10.2 | 1 | 11.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 6.2 | 10.2 | 1 | 11 | ns |
| $t_{PLZ}$* | | | | | 6.2 | 10.2 | 1 | 11 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.4 | 10.4 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.4 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7.3 | 11.2 | 1 | 12.5 | ns |
| $t_{PZL}$ | | | | | 7.3 | 11.2 | 1 | 12.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7 | 11.2 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 7 | 11.2 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended free-air temperature operating range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT374 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 90 | 140 | | 80 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 130 | | 75 | | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 5.6 | 9.4 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 9.4 | 1 | 10.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 6.5 | 10.2 | 1 | 11.5 | ns |
| $t_{PZL}$ | | | | | 6.5 | 10.2 | 1 | 11.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 6.2 | 10.2 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 6.2 | 10.2 | 1 | 11 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.4 | 10.4 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.4 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7.3 | 11.2 | 1 | 12.5 | ns |
| $t_{PZL}$ | | | | | 7.3 | 11.2 | 1 | 12.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7 | 11.2 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 7 | 11.2 | 1 | 12 | |

## output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT374 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

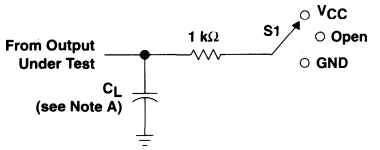
| PARAMETER | | SN74AHCT374 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | 1.2 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | –1.2 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 3.8 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

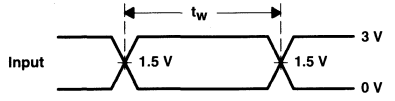
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 27 | pF |

## PARAMETER MEASUREMENT INFORMATION

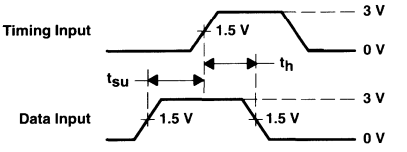



LOAD CIRCUIT

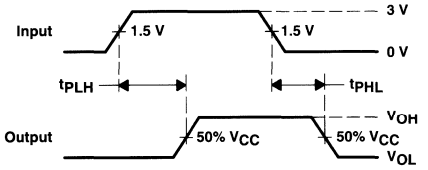
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



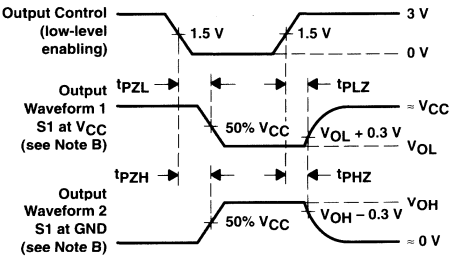

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES



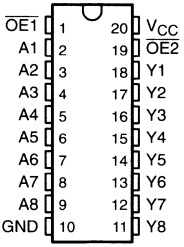

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

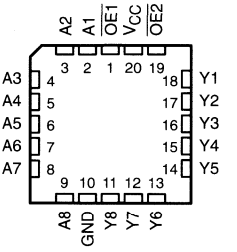
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC540 . . . J OR W PACKAGE**
**SN74AHC540 . . . DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC540 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHC540 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

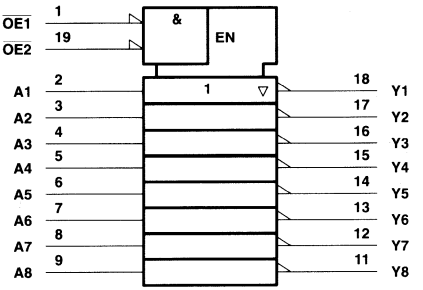
The SN54AHC540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC540 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each buffer/driver)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

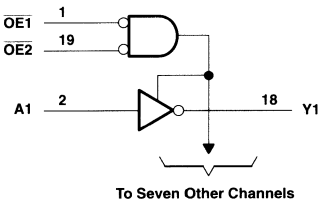
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC540 | | SN74AHC540 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC540 | | SN74AHC540 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | Data inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| | Control inputs | | | | | ±0.1 | | ±1 | | ±1 | |
| $I_{OZ}$† | | $V_O$ = $V_{CC}$ or GND, $V_I$ ($\overline{OE}$) = $V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| $C_o$ | | $V_O$ = $V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

† For I/O pins, the parameter $I_{OZ}$ includes the input leakage current.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC540 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 4.8 | 7 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 4.8 | 7 | 1 | 8.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6.8 | 10.5 | 1 | 12.5 | ns |
| $t_{PZL}$* | | | | | 6.8 | 10.5 | 1 | 12.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6.8 | 10.5 | 1 | 12.5 | ns |
| $t_{PLZ}$* | | | | | 6.8 | 10.5 | 1 | 12.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.3 | 10.5 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.3 | 10.5 | 1 | 12 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8 | 14 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 8 | 14 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8 | 15.4 | 1 | 17.5 | ns |
| $t_{PLZ}$ | | | | | 8 | 15.4 | 1 | 17.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC540 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 4.8 | 7 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 4.8 | 7 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6.8 | 10.5 | 1 | 12.5 | ns |
| $t_{PZL}$ | | | | | 6.8 | 10.5 | 1 | 12.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6.8 | 10.5 | 1 | 12.5 | ns |
| $t_{PLZ}$ | | | | | 6.8 | 10.5 | 1 | 12.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.3 | 10.5 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.3 | 10.5 | 1 | 12 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8 | 14 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 8 | 14 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8 | 15.4 | 1 | 17.5 | ns |
| $t_{PLZ}$ | | | | | 8 | 15.4 | 1 | 17.5 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC540 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.7 | 5 | 1 | 6 | ns |
| $t_{PHL}$* | | | | | 3.7 | 5 | 1 | 6 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.7 | 7.2 | 1 | 8.5 | ns |
| $t_{PZL}$* | | | | | 4.7 | 7.2 | 1 | 8.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.5 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$* | | | | | 4.5 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.2 | 7 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5.2 | 7 | 1 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 9.2 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 6.2 | 9.2 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6 | 8.8 | 1 | 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC540 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.7 | 5 | 1 | 6 | ns |
| $t_{PHL}$ | | | | | 3.7 | 5 | 1 | 6 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.7 | 7.2 | 1 | 8.5 | ns |
| $t_{PZL}$ | | | | | 4.7 | 7.2 | 1 | 8.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.5 | 6.8 | 1 | 8 | ns |
| $t_{PLZ}$ | | | | | 4.5 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.2 | 7 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5.2 | 7 | 1 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 9.2 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 6.2 | 9.2 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6 | 8.8 | 1 | 10 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74AHC540 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | | MIN | MAX | | | |
| $t_{sk(o)}$ | A | Y | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

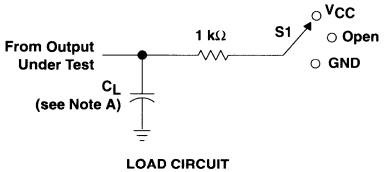
| PARAMETER | | SN74AHC540 MIN | SN74AHC540 MAX | UNIT |
|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.7 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

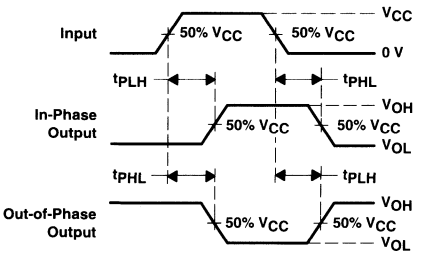
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 12 | pF |

## PARAMETER MEASUREMENT INFORMATION

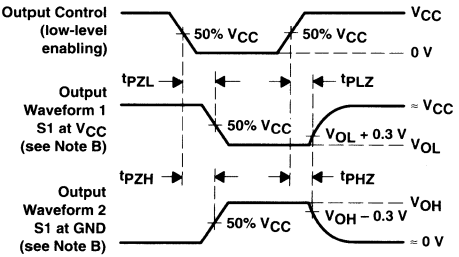



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



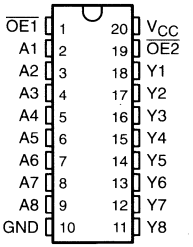

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

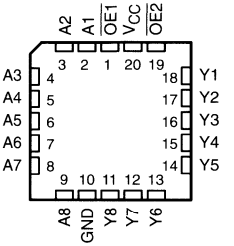
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT540 . . . J OR W PACKAGE**
**SN74AHCT540 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT540 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHCT540 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

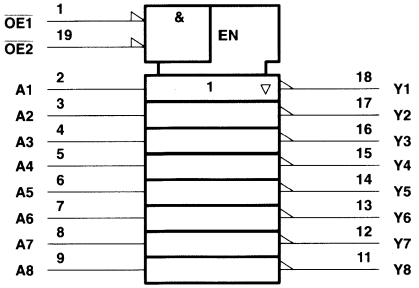
The SN54AHCT540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT540 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

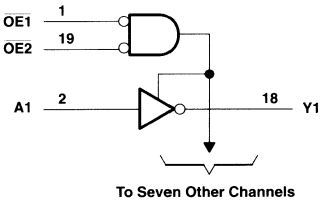
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DGV package ..... 146°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT540 | | SN74AHCT540 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT540 | | SN74AHCT540 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT540 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 4 | 6 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 4 | 6 | 1 | 7.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.5 | 8 | 1 | 9 | ns |
| $t_{PZL}$* | | | | | 5.5 | 8 | 1 | 9 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 8 | 1 | 9 | ns |
| $t_{PLZ}$* | | | | | 5 | 8 | 1 | 9 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 6 | 8.5 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 6 | 8.5 | 1 | 10 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 7.5 | 11 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.5 | 11 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8 | 11 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 8 | 11 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT540 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 4 | 6 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 4 | 6 | 1 | 7.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.5 | 8 | 1 | 9 | ns |
| $t_{PZL}$ | | | | | 5.5 | 8 | 1 | 9 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 8 | 1 | 9 | ns |
| $t_{PLZ}$ | | | | | 5 | 8 | 1 | 9 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 6 | 8.5 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 6 | 8.5 | 1 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.5 | 11 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.5 | 11 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8 | 11 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 8 | 11 | 1 | 12 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74AHCT540 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | | MIN | MAX | | | |
| $t_{sk(o)}$ | A | Y | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

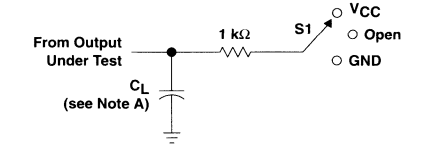
| PARAMETER | | SN74AHCT540 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

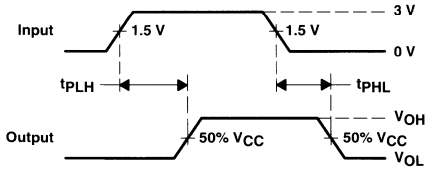
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 12 | pF |

## PARAMETER MEASUREMENT INFORMATION

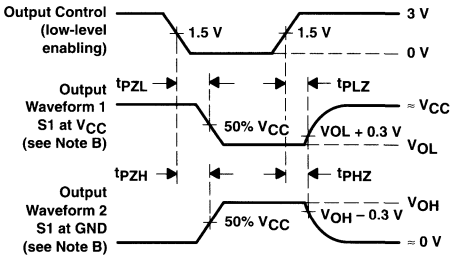



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



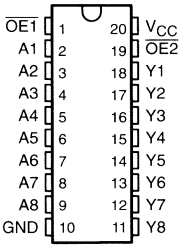

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

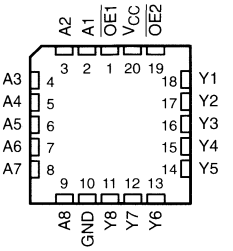
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC541 . . . J OR W PACKAGE**
**SN74AHC541 . . . DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC541 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHC541 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

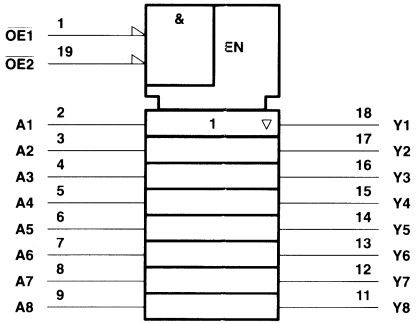
The SN54AHC541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC541 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each buffer/driver)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

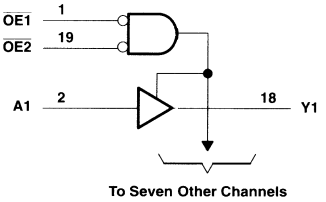
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC541 | | SN74AHC541 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC541 | | SN74AHC541 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | Data inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| | Control inputs | | | | | ±0.1 | | ±1 | | ±1 | |
| $I_{OZ}$† | | $V_O$ = $V_{CC}$ or GND, $V_I$ ($\overline{OE}$) = $V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| $C_o$ | | $V_O$ = $V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

† For input and ouput, $I_{OZ}$ includes the input leakage current.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC541 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5 | 7 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5 | 7 | 1 | 8.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6 | 10.5 | 1 | 11 | ns |
| $t_{PZL}$* | | | | | 6 | 10.5 | 1 | 11 | |
| $t_{PHZ}$* | OE | Y | $C_L$ = 15 pF | | 7 | 11 | 1 | 12 | ns |
| $t_{PLZ}$* | | | | | 7 | 11 | 1 | 12 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.5 | 10.5 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.5 | 10.5 | 1 | 12 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 8 | 14 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 8 | 14 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 9 | 15.4 | 1 | 17.5 | ns |
| $t_{PLZ}$ | | | | | 9 | 15.4 | 1 | 17.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC541 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5 | 7 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5 | 7 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6 | 10.5 | 1 | 11 | ns |
| $t_{PZL}$ | | | | | 6 | 10.5 | 1 | 11 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 15 pF | | 7 | 11 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 7 | 11 | 1 | 12 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.5 | 10.5 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.5 | 10.5 | 1 | 12 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8 | 14 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 8 | 14 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 9 | 15.4 | 1 | 17.5 | ns |
| $t_{PLZ}$ | | | | | 9 | 15.4 | 1 | 17.5 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC541 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.5 | 5 | 1 | 6 | ns |
| $t_{PHL}$* | | | | | 3.5 | 5 | 1 | 6 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.7 | 7.2 | 1 | 8.5 | ns |
| $t_{PZL}$* | | | | | 4.7 | 7.2 | 1 | 8.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 7.5 | 1 | 8 | ns |
| $t_{PLZ}$* | | | | | 5 | 7.5 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5 | 7 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 7 | 1 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 9.2 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 6.2 | 9.2 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6 | 8.8 | 1 | 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC541 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.5 | 5 | 1 | 6 | ns |
| $t_{PHL}$ | | | | | 3.5 | 5 | 1 | 6 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.7 | 7.2 | 1 | 8.5 | ns |
| $t_{PZL}$ | | | | | 4.7 | 7.2 | 1 | 8.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 7.5 | 1 | 8 | ns |
| $t_{PLZ}$ | | | | | 5 | 7.5 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5 | 7 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 7 | 1 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 9.2 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 6.2 | 9.2 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6 | 8.8 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6 | 8.8 | 1 | 10 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74AHC541 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | | MIN | MAX | | | |
| $t_{sk(o)}$ | A | Y | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

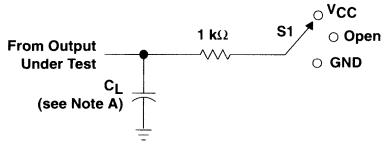
| PARAMETER | | SN74AHC541 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.7 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

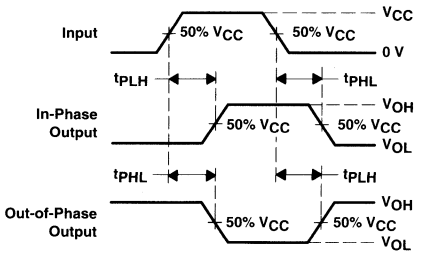
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 12 | pF |

## PARAMETER MEASUREMENT INFORMATION

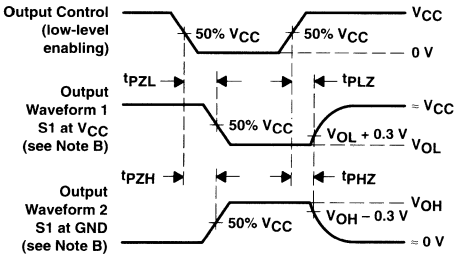



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



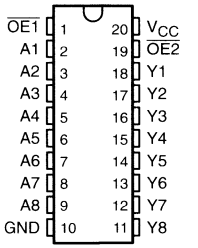

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

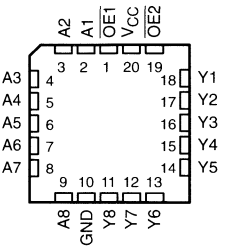
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT541 . . . J OR W PACKAGE**
**SN74AHCT541 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT541 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHCT541 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

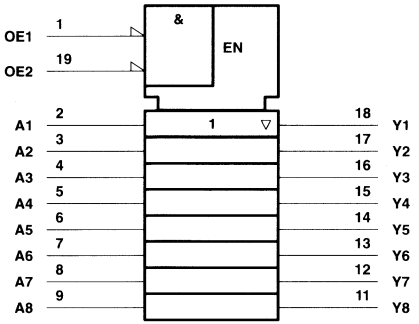
The SN54AHCT541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT541 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

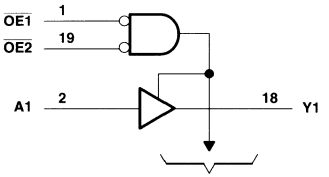
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I < 0$) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DGV package ..... 146°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT541 | | SN74AHCT541 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT541 | | SN74AHCT541 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT541 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 4.1 | 6 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.7 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 7 | 1 | 8 | ns |
| $t_{PZL}$* | | | | | 5 | 7 | 1 | 8 | |
| $t_{PHZ}$* | OE | Y | $C_L$ = 15 pF | | 4.5 | 7 | 1 | 8 | ns |
| $t_{PLZ}$* | | | | | 4.5 | 7 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 6.2 | 8.5 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 6 | 8.5 | 1 | 9.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 7.5 | 10 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.5 | 10 | 1 | 12 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 7 | 10 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 7 | 10 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT541 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 4.1 | 6 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 3.7 | 5.5 | 1 | 6.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 7 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 5 | 7 | 1 | 8 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 15 pF | | 4.5 | 7 | 1 | 8 | ns |
| $t_{PLZ}$ | | | | | 4.5 | 7 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 6.2 | 8.5 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 6 | 8.5 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.5 | 10 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.5 | 10 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7 | 10 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 7 | 10 | 1 | 12 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74AHCT541 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | | MIN | MAX | | | |
| $t_{sk(o)}$ | A | Y | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

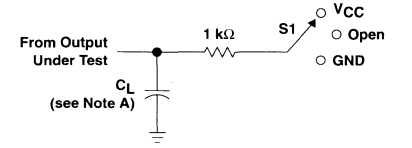
| PARAMETER | | SN74AHCT541 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

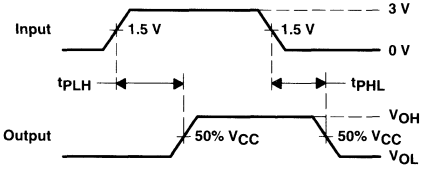
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 12 | pF |

## PARAMETER MEASUREMENT INFORMATION

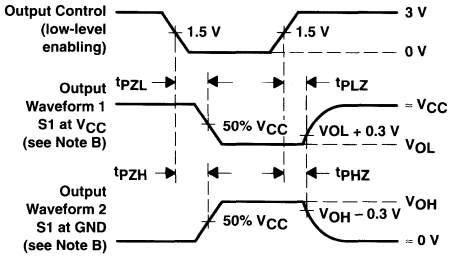



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



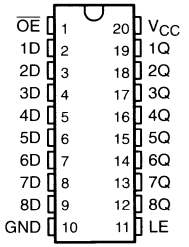

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

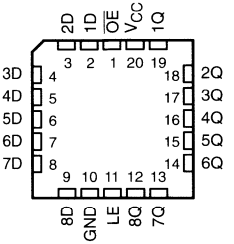
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- **3-State Outputs Directly Drive Bus Lines**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC573 . . . J OR W PACKAGE**
**SN74AHC573 . . . DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC573 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHC573 are octal transparent D-type latches.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

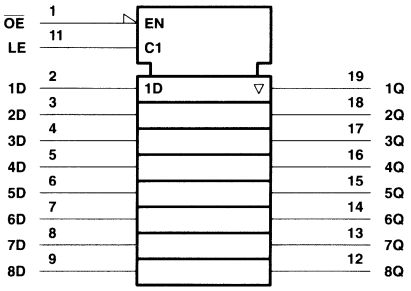
The SN54AHC573 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC573 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

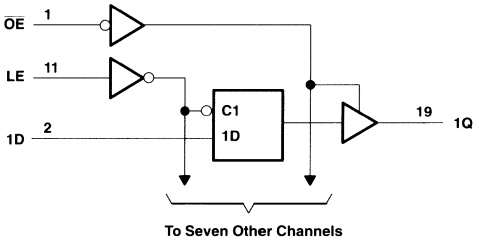
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC573 | | SN74AHC573 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC573 | | SN74AHC573 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{OZ}$ | $V_I$ = $V_{IL}$ or $V_{IH}$, $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 3.5 | | | | | | pF |

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| | | $T_A$ = 25°C | | SN54AHC573 | | SN74AHC573 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 3.5 | | 3.5 | | 3.5 | | ns |
| $t_h$ | Hold time, data after LE↓ | 1.5 | | 1.5 | | 1.5 | | ns |

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| | | $T_A$ = 25°C | | SN54AHC573 | | SN74AHC573 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 3.5 | | 3.5 | | 3.5 | | ns |
| $t_h$ | Hold time, data after LE↓ | 1.5 | | 1.5 | | 1.5 | | ns |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC573 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | D | Q | $C_L$ = 15 pF | | 7 | 11 | 1 | 13 | ns |
| $t_{PHL}$* | | | | | 7 | 11 | 1 | 13 | |
| $t_{PLH}$* | LE | Q | $C_L$ = 15 pF | | 7.6 | 11.9 | 1 | 14 | ns |
| $t_{PHL}$* | | | | | 7.6 | 11.9 | 1 | 14 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.3 | 11.5 | 1 | 13.5 | ns |
| $t_{PZL}$* | | | | | 7.3 | 11.5 | 1 | 13.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 8.3 | 11 | 1 | 13 | ns |
| $t_{PLZ}$* | | | | | 8.3 | 11 | 1 | 13 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 9.5 | 14.5 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | | 9.5 | 14.5 | 1 | 16.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 10.1 | 15.4 | 1 | 17.5 | ns |
| $t_{PHL}$ | | | | | 10.1 | 15.4 | 1 | 17.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.8 | 15 | 1 | 17 | ns |
| $t_{PZL}$ | | | | | 9.8 | 15 | 1 | 17 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 10.7 | 14.5 | 1 | 16.5 | ns |
| $t_{PLZ}$ | | | | | 10.7 | 14.5 | 1 | 16.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC573 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | D | Q | $C_L$ = 15 pF | | 7 | 11 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 7 | 11 | 1 | 13 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 15 pF | | 7.6 | 11.9 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 7.6 | 11.9 | 1 | 14 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.3 | 11.5 | 1 | 13.5 | ns |
| $t_{PZL}$ | | | | | 7.3 | 11.5 | 1 | 13.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 8.3 | 11 | 1 | 13 | ns |
| $t_{PLZ}$ | | | | | 8.3 | 11 | 1 | 13 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 9.5 | 14.5 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | | 9.5 | 14.5 | 1 | 16.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 10.1 | 15.4 | 1 | 17.5 | ns |
| $t_{PHL}$ | | | | | 10.1 | 15.4 | 1 | 17.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.8 | 15 | 1 | 17 | ns |
| $t_{PZL}$ | | | | | 9.8 | 15 | 1 | 17 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 10.7 | 14.5 | 1 | 16.5 | ns |
| $t_{PLZ}$ | | | | | 10.7 | 14.5 | 1 | 16.5 | |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC573 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | D | Q | $C_L$ = 15 pF | | 4.5 | 6.8 | 1 | 8 | ns |
| $t_{PHL}$* | | | | | 4.5 | 6.8 | 1 | 8 | |
| $t_{PLH}$* | LE | Q | $C_L$ = 15 pF | | 5 | 7.7 | 1 | 9 | ns |
| $t_{PHL}$* | | | | | 5 | 7.7 | 1 | 9 | |
| $t_{PZH}$* | OE | Q | $C_L$ = 15 pF | | 5.2 | 7.7 | 1 | 9 | ns |
| $t_{PZL}$* | | | | | 5.2 | 7.7 | 1 | 9 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.2 | 7.7 | 1 | 9 | ns |
| $t_{PLZ}$* | | | | | 5.2 | 7.7 | 1 | 9 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 6 | 8.8 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 6 | 8.8 | 1 | 10 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 6.5 | 9.7 | 1 | 11 | ns |
| $t_{PHL}$ | | | | | 6.5 | 9.7 | 1 | 11 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.7 | 9.7 | 1 | 11 | ns |
| $t_{PZL}$ | | | | | 6.7 | 9.7 | 1 | 11 | |
| $t_{PHZ}$ | OE | Q | $C_L$ = 50 pF | | 6.7 | 9.7 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 6.7 | 9.7 | 1 | 11 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC573 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | D | Q | $C_L$ = 15 pF | | 4.5 | 6.8 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 4.5 | 6.8 | 1 | 8 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 15 pF | | 5 | 7.7 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 5 | 7.7 | 1 | 9 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.2 | 7.7 | 1 | 9 | ns |
| $t_{PZL}$ | | | | | 5.2 | 7.7 | 1 | 9 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.2 | 7.7 | 1 | 9 | ns |
| $t_{PLZ}$ | | | | | 5.2 | 7.7 | 1 | 9 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 6 | 8.8 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 6 | 8.8 | 1 | 10 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 6.5 | 9.7 | 1 | 11 | ns |
| $t_{PHL}$ | | | | | 6.5 | 9.7 | 1 | 11 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.7 | 9.7 | 1 | 11 | ns |
| $t_{PZL}$ | | | | | 6.7 | 9.7 | 1 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.7 | 9.7 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 6.7 | 9.7 | 1 | 11 | |

## output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC573 | | UNIT |
|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | MIN MAX | |
| | | | MIN MAX | | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | 1.5 | 1.5 | ns |
| | | 5 V ± 0.5 V | 1 | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

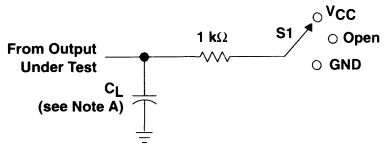
| PARAMETER | | SN74AHC573 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 1 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

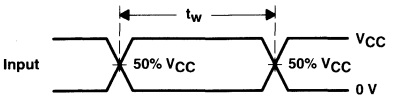
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 16 | pF |

## PARAMETER MEASUREMENT INFORMATION

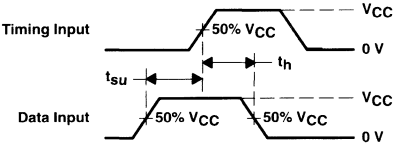



LOAD CIRCUIT

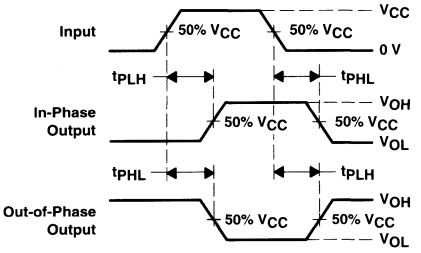
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



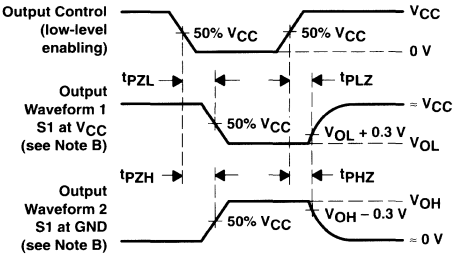

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES



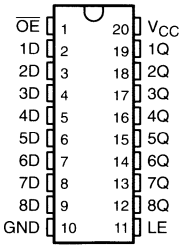

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

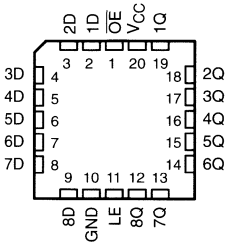
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT573 . . . J OR W PACKAGE**
**SN74AHCT573 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT573 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHCT573 are octal-transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

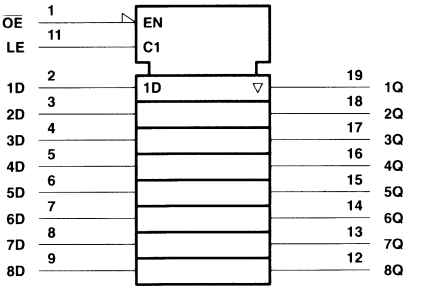
The SN54AHCT573 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT573 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

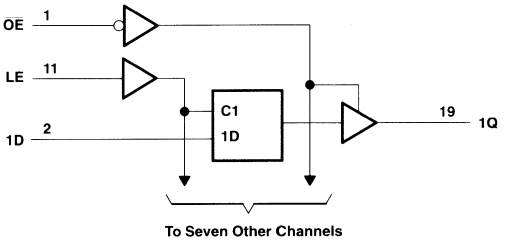
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DGV package ..... 146°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT573 | | SN74AHCT573 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT573 | | SN74AHCT573 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 3 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHCT573 | | SN74AHCT573 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 3.5 | | 3.5 | | 3.5 | | ns |
| $t_h$ | Hold time, data after LE↓ | 1.5 | | 1.5 | | 1.5 | | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT573 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | D | Q | $C_L$ = 15 pF | | 4.2 | 6 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 5.1 | 7 | 1 | 9 | |
| $t_{PLH}$* | LE | Q | $C_L$ = 15 pF | | 4.7 | 6.5 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 5.6 | 7.5 | 1 | 9 | |
| $t_{PZH}$* | OE | Q | $C_L$ = 15 pF | | 4.1 | 6.5 | 1 | 7 | ns |
| $t_{PZL}$* | | | | | 5.5 | 7.5 | 1 | 10 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.5 | 8 | 1 | 11 | ns |
| $t_{PLZ}$* | | | | | 5.4 | 8 | 1 | 9.5 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 5.2 | 7 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 6.1 | 8 | 1 | 10 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 5.7 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 6.6 | 8.5 | 1 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 5.1 | 7.5 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 6.5 | 8.5 | 1 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.7 | 9 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 6.4 | 9 | 1 | 10.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT573 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | D | Q | $C_L$ = 15 pF | | 4.2 | 6 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 5.1 | 7 | 1 | 9 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 15 pF | | 4.7 | 6.5 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 7.5 | 1 | 9 | |
| $t_{PZH}$ | OE | Q | $C_L$ = 15 pF | | 4.1 | 6.5 | 1 | 7 | ns |
| $t_{PZL}$ | | | | | 5.5 | 7.5 | 1 | 10 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.5 | 8 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 5.4 | 8 | 1 | 9.5 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 5.2 | 7 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 6.1 | 8 | 1 | 10 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 5.7 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 6.6 | 8.5 | 1 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 5.1 | 7.5 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 6.5 | 8.5 | 1 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.7 | 9 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 6.4 | 9 | 1 | 10.5 | |

## output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT573 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

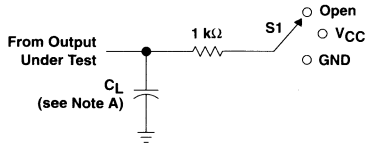
| PARAMETER | | SN74AHCT573 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

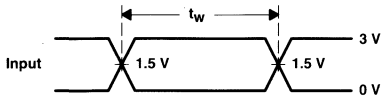
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 16 | pF |

## PARAMETER MEASUREMENT INFORMATION

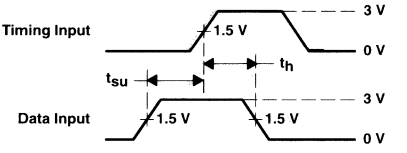



LOAD CIRCUIT

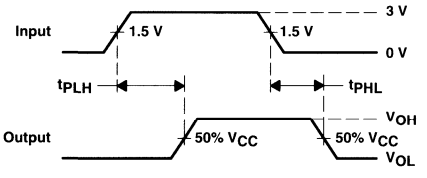
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



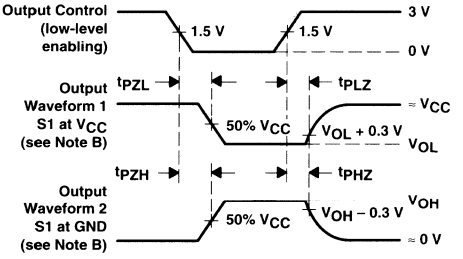

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES



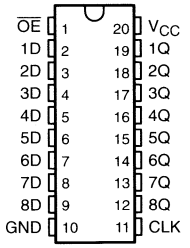

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

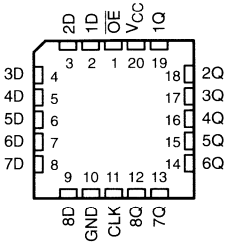
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- **3-State Outputs Drive Bus Lines Directly**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC574 . . . J OR W PACKAGE**
**SN74AHC574 . . . DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC574 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHC574 are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

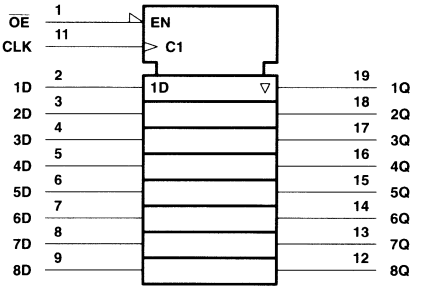
The SN54AHC574 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC574 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each flip-flop)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

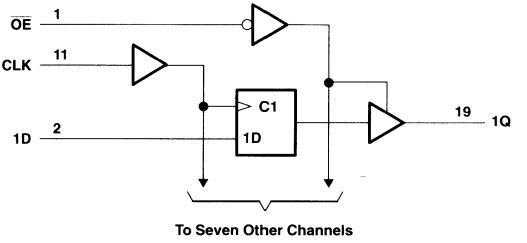
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I < 0$) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54AHC574 | | SN74AHC574 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC574 | | SN74AHC574 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 3 | 10 | | | | 10 | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 3 | | | | | | pF |

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| | | $T_A$ = 25°C | | SN54AHC574 | | SN74AHC574 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 3.5 | | 3.5 | | 3.5 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 1.5 | | 1.5 | | 1.5 | | ns |

**timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| | | $T_A$ = 25°C | | SN54AHC574 | | SN74AHC574 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 3 | | 3 | | 3 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 1.5 | | 1.5 | | 1.5 | | ns |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC574 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 80 | 125 | | 65 | | MHz |
| | | | $C_L$ = 50 pF | 50 | 75 | | 45 | | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 8.5 | 13.2 | 1 | 15.5 | ns |
| $t_{PHL}$* | | | | | 8.5 | 13.2 | 1 | 15.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 8.2 | 12.8 | 1 | 15 | ns |
| $t_{PZL}$* | | | | | 8.2 | 12.8 | 1 | 15 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 8.5 | 13 | 1 | 15 | ns |
| $t_{PLZ}$* | | | | | 8.5 | 13 | 1 | 15 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 11 | 16.7 | 1 | 19 | ns |
| $t_{PHL}$ | | | | | 11 | 16.7 | 1 | 19 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 10.7 | 16.3 | 1 | 18.5 | ns |
| $t_{PZL}$ | | | | | 10.7 | 16.3 | 1 | 18.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 11 | 15 | 1 | 17 | ns |
| $t_{PLZ}$ | | | | | 11 | 15 | 1 | 17 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC574 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 80 | 125 | | 65 | | MHz |
| | | | $C_L$ = 50 pF | 50 | 75 | | 45 | | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 8.5 | 13.2 | 1 | 15.5 | ns |
| $t_{PHL}$ | | | | | 8.5 | 13.2 | 1 | 15.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 8.2 | 12.8 | 1 | 15 | ns |
| $t_{PZL}$ | | | | | 8.2 | 12.8 | 1 | 15 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 8.5 | 13 | 1 | 15 | ns |
| $t_{PLZ}$ | | | | | 8.5 | 13 | 1 | 15 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 11 | 16.7 | 1 | 19 | ns |
| $t_{PHL}$ | | | | | 11 | 16.7 | 1 | 19 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 10.7 | 16.3 | 1 | 18.5 | ns |
| $t_{PZL}$ | | | | | 10.7 | 16.3 | 1 | 18.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 11 | 15 | 1 | 17 | ns |
| $t_{PLZ}$ | | | | | 11 | 15 | 1 | 17 | |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC574 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 130 | 180 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 115 | | 75 | | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PZH}$* | OE | Q | $C_L$ = 15 pF | | 5.9 | 9 | 1 | 10.5 | ns |
| $t_{PZL}$* | | | | | 5.9 | 9 | 1 | 10.5 | |
| $t_{PHZ}$* | OE | Q | $C_L$ = 15 pF | | 5.5 | 9 | 1 | 10.5 | ns |
| $t_{PLZ}$* | | | | | 5.5 | 9 | 1 | 10.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |
| $t_{PZH}$ | OE | Q | $C_L$ = 50 pF | | 7.4 | 11 | 1 | 12.5 | ns |
| $t_{PZL}$ | | | | | 7.4 | 11 | 1 | 12.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7.1 | 10.1 | 1 | 11.5 | ns |
| $t_{PLZ}$ | | | | | 7.1 | 10.1 | 1 | 11.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC574 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 130 | 180 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 115 | | 75 | | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 5.6 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8.6 | 1 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.9 | 9 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 5.9 | 9 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.5 | 9 | 1 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 5.5 | 9 | 1 | 10.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.6 | 1 | 12 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7.4 | 11 | 1 | 12.5 | ns |
| $t_{PZL}$ | | | | | 7.4 | 11 | 1 | 12.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7.1 | 10.1 | 1 | 11.5 | ns |
| $t_{PLZ}$ | | | | | 7.1 | 10.1 | 1 | 11.5 | |

## output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC574 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

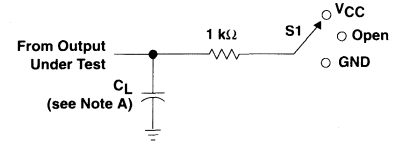
| PARAMETER | | SN74AHC574 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.2 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

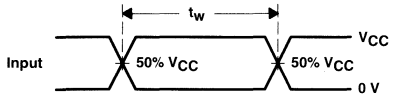
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 28 | pF |

## PARAMETER MEASUREMENT INFORMATION

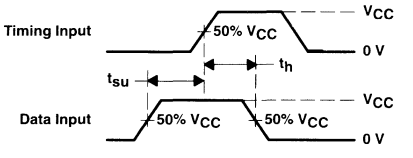



LOAD CIRCUIT

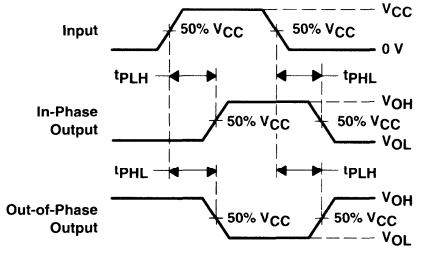
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



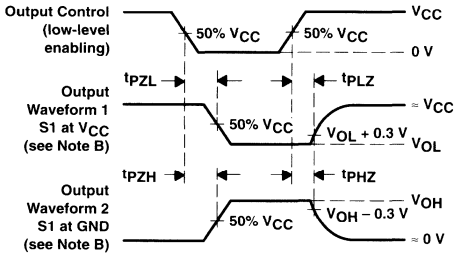

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES



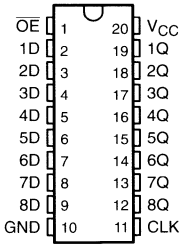

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

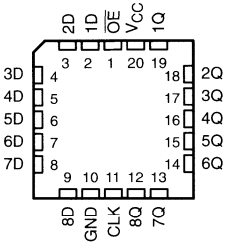
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT574 . . . J OR W PACKAGE**
**SN74AHCT574 . . . DB, DGV, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT574 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'AHCT574 are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

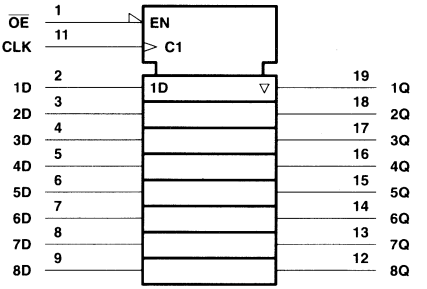
The SN54AHCT574 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT574 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each flip-flop)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

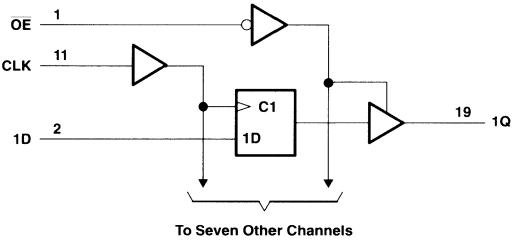
EPIC is a trademark of Texas Instruments Incorporated.

### logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package ..... 115°C/W
DGV package ..... 146°C/W
DW package ..... 97°C/W
N package ..... 67°C/W
PW package ..... 128°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT574 | | SN74AHCT574 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT574 | | SN74AHCT574 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 3 | 10 | | | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 3 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHCT574 | | SN74AHCT574 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 5 | | 5.5 | | 5.5 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 3 | | 3.5 | | 3.5 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 1.5 | | 1.5 | | 1.5 | | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT574 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 130 | 180 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 115 | | 75 | | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 5.5 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 5.5 | 8.6 | 1 | 10 | |
| $t_{PZH}$* | OE | Q | $C_L$ = 15 pF | | 5 | 9 | 1 | 10.5 | ns |
| $t_{PZL}$* | | | | | 5 | 9 | 1 | 10.5 | |
| $t_{PHZ}$* | OE | Q | $C_L$ = 15 pF | | 5.5 | 9 | 1 | 10.5 | ns |
| $t_{PLZ}$* | | | | | 5.5 | 9 | 1 | 10.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 7 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7 | 10.6 | 1 | 12 | |
| $t_{PZH}$ | OE | Q | $C_L$ = 50 pF | | 6 | 11 | 1 | 12.5 | ns |
| $t_{PZL}$ | | | | | 6 | 11 | 1 | 12.5 | |
| $t_{PHZ}$ | OE | Q | $C_L$ = 50 pF | | 7 | 10.1 | 1 | 11.5 | ns |
| $t_{PLZ}$ | | | | | 7 | 10.1 | 1 | 11.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT574 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 130 | 180 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 115 | | 75 | | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 5.5 | 8.6 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 5.5 | 8.6 | 1 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5 | 9 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 5 | 9 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.5 | 9 | 1 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 5.5 | 9 | 1 | 10.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 7 | 10.6 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7 | 10.6 | 1 | 12 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6 | 11 | 1 | 12.5 | ns |
| $t_{PZL}$ | | | | | 6 | 11 | 1 | 12.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7 | 10.1 | 1 | 11.5 | ns |
| $t_{PLZ}$ | | | | | 7 | 10.1 | 1 | 11.5 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT574 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

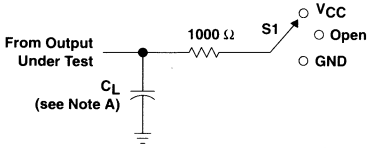
| PARAMETER | | SN74AHCT574 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

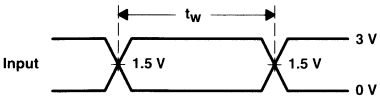
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 28 | pF |

## PARAMETER MEASUREMENT INFORMATION

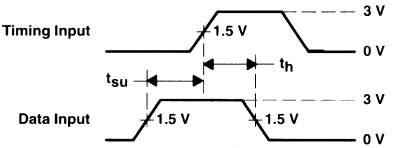



LOAD CIRCUIT

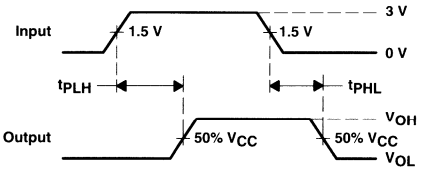
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



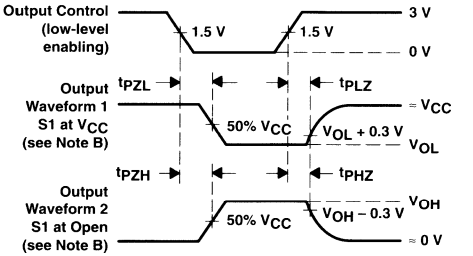

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES



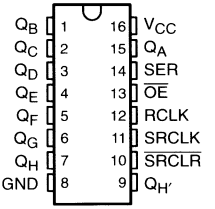

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

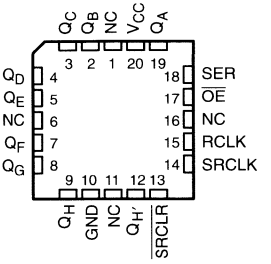
**Figure 1. Load Circuit and Voltage Waveforms**

- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **8-Bit Serial-In, Parallel-Out Shift**
- **Shift Register Has Direct Clear**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHC595 . . . J OR W PACKAGE**
**SN74AHC595 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC595 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHC595 contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and serial outputs for cascading. When the output-enable ($\overline{OE}$) input is high, the outputs are in the high-impedance state.

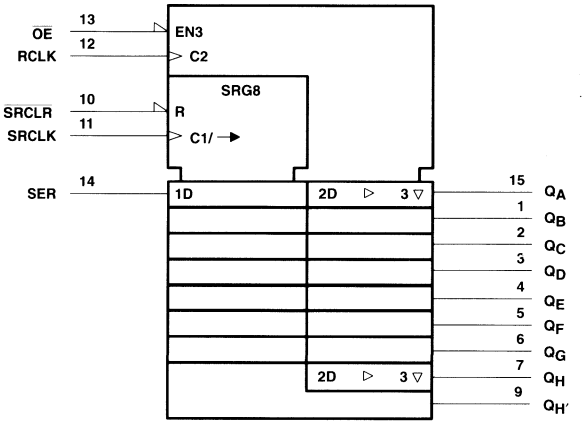
Both the shift register clock (RCLK) and storage register clock (SRCLK) are positive-edge triggered. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

The SN54AHC595 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC595 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

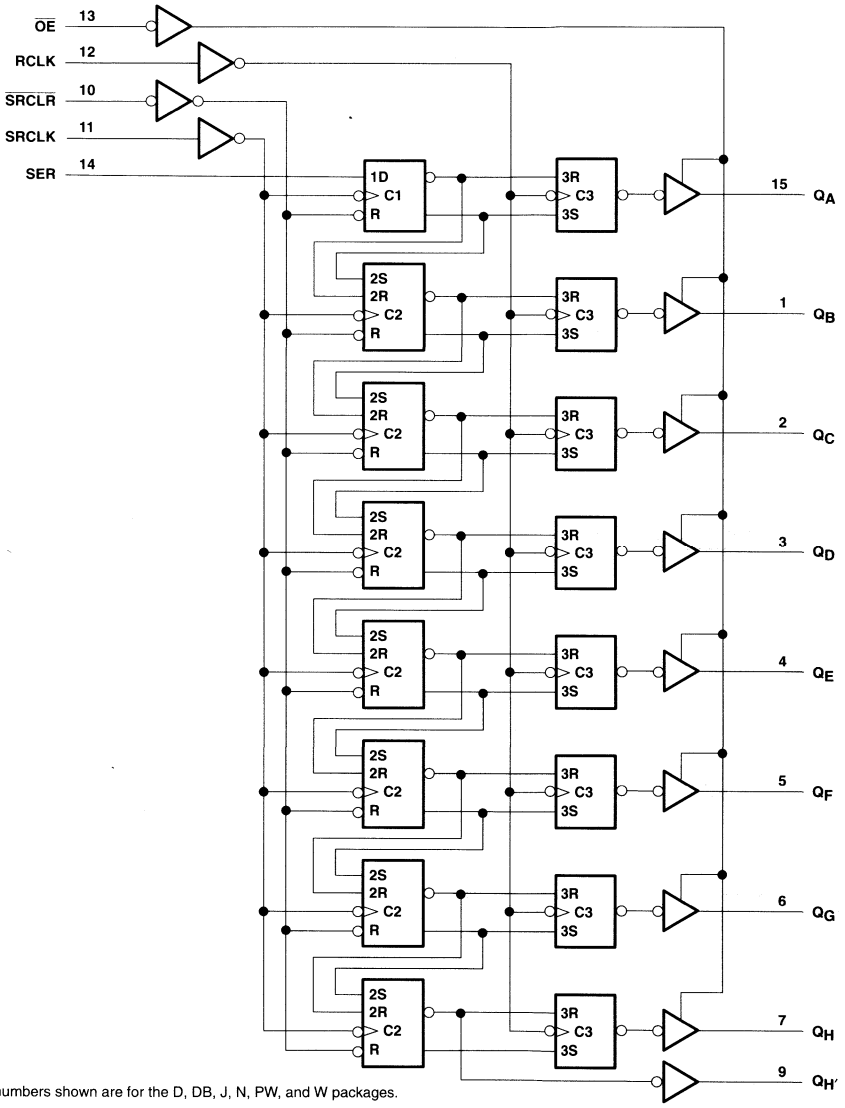
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

### absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | | SN54AHC595 | | SN74AHC595 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC595 | | SN74AHC595 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{OZ}$ | $V_I = V_{CC}$ or GND, $V_O = V_{CC}$ or GND, $\overline{OE} = V_{IH}$ or $V_{IL}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHC595 | | SN74AHC595 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | SRCLK high or low | 5 | | 5 | | 5 | | ns |
| | | RCLK high or low | 5 | | 5 | | 5 | | |
| | | SRCLR low | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time | SER before SRCLK↑ | 3.5 | | 3.5 | | 3.5 | | ns |
| | | SRCLK↑ before RCLK↑† | 8 | | 8.5 | | 8.5 | | |
| | | SRCLR low before RCLK↑ | 8 | | 9 | | 9 | | |
| | | SRCLR high (inactive) before SRCLK↑ | 3 | | 3 | | 3 | | |
| $t_h$ | Hold time | SER after SRCLK↑ | 1.5 | | 1.5 | | 1.5 | | ns |
| | | SRCLK↑ after RCLK↑ | 0 | | 0 | | 0 | | |
| | | SRCLR low after RCLK↑ | 0 | | 0 | | 0 | | |

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

PRODUCT PREVIEW

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHC595 | | SN74AHC595 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ Pulse duration | SRCLK high or low | 5 | | 5 | | 5 | | ns |
| | RCLK high or low | 5 | | 5 | | 5 | | |
| | SRCLR low | 5 | | 5 | | 5 | | |
| $t_{su}$ Setup time | SER before SRCLK↑ | 3 | | 3 | | 3 | | ns |
| | SRCLK↑ before RCLK↑† | 5 | | 5 | | 5 | | |
| | SRCLR low before RCLK↑ | 5 | | 5 | | 5 | | |
| | SRCLR high (inactive) before SRCLK↑ | 2.5 | | 2.5 | | 2.5 | | |
| $t_h$ Hold time | SER after SRCLK↑ | 2 | | 2 | | 2 | | ns |
| | SRCLK↑ after RCLK↑ | 0 | | 0 | | 0 | | |
| | SRCLR low after RCLK↑ | 0 | | 0 | | 0 | | |

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

PRODUCT PREVIEW

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC595 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 80 | 150 | | 70 | | MHz |
| | | | $C_L$ = 50 pF | 55 | 130 | | 50 | | |
| $t_{PLH}$* | RCLK | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 7.7 | 11.9 | 1 | 13.5 | ns |
| $t_{PHL}$* | | | | | 7.7 | 11.9 | 1 | 13.5 | |
| $t_{PLH}$* | SRCLK | $Q_{H'}$ | $C_L$ = 15 pF | | 8.8 | 13 | 1 | 15 | ns |
| $t_{PHL}$* | | | | | 8.8 | 13 | 1 | 15 | |
| $t_{PHL}$* | SRCLR | $Q_{H'}$ | $C_L$ = 15 pF | | 8.4 | 12.8 | 1 | 13.7 | ns |
| $t_{PZH}$* | OE | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 7.5 | 11.5 | 1 | 13.5 | ns |
| $t_{PZL}$* | | | | | 7.5 | 11.5 | 1 | 13.5 | |
| $t_{PHZ}$* | OE | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$* | | | | | | | | | |
| $t_{PLH}$ | RCLK | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 10.2 | 15.4 | 1 | 17 | ns |
| $t_{PHL}$ | | | | | 10.2 | 15.4 | 1 | 17 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | $C_L$ = 50 pF | | 11.3 | 16.5 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 11.3 | 16.5 | 1 | 18.5 | |
| $t_{PHL}$ | SRCLR | $Q_{H'}$ | $C_L$ = 50 pF | | 10.9 | 16.3 | 1 | 17.2 | ns |
| $t_{PZH}$ | OE | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 9 | 15 | 1 | 17 | ns |
| $t_{PZL}$ | | | | | 9 | 15 | 1 | 17 | |
| $t_{PHZ}$ | OE | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 12.1 | 15.7 | 1 | 16.2 | ns |
| $t_{PLZ}$ | | | | | 12.1 | 15.7 | 1 | 16.2 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC595 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 80 | 150 | | 70 | | MHz |
| | | | $C_L$ = 50 pF | 55 | 130 | | 50 | | |
| $t_{PLH}$ | RCLK | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 7.7 | 11.9 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 7.7 | 11.9 | 1 | 13.5 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | $C_L$ = 15 pF | | 8.8 | 13 | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.8 | 13 | 1 | 15 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | $C_L$ = 15 pF | | 8.4 | 12.8 | 1 | 13.7 | ns |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 7.5 | 11.5 | 1 | 13.5 | ns |
| $t_{PZL}$ | | | | | 7.5 | 11.5 | 1 | 13.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |
| $t_{PLH}$ | RCLK | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 10.2 | 15.4 | 1 | 17 | ns |
| $t_{PHL}$ | | | | | 10.2 | 15.4 | 1 | 17 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | $C_L$ = 50 pF | | 11.3 | 16.5 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 11.3 | 16.5 | 1 | 18.5 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | $C_L$ = 50 pF | | 10.9 | 16.3 | 1 | 17.2 | ns |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 9 | 15 | 1 | 17 | ns |
| $t_{PZL}$ | | | | | 9 | 15 | 1 | 17 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 12.1 | 15.7 | 1 | 16.2 | ns |
| $t_{PLZ}$ | | | | | 12.1 | 15.7 | 1 | 16.2 | |

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHC595 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 135 | 185 | | 115 | | MHz |
| | | | $C_L$ = 50 pF | 95 | 155 | | 85 | | |
| $t_{PLH}$* | RCLK | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 5.4 | 7.4 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5.4 | 7.4 | 1 | 8.5 | |
| $t_{PLH}$* | SRCLK | $Q_{H'}$ | $C_L$ = 15 pF | | 6.2 | 8.2 | 1 | 9.4 | ns |
| $t_{PHL}$* | | | | | 6.2 | 8.2 | 1 | 9.4 | |
| $t_{PHL}$* | SRCLR | $Q_{H'}$ | $C_L$ = 15 pF | | 5.9 | 8 | 1 | 9.1 | ns |
| $t_{PZH}$* | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 4.8 | 8.6 | 1 | 10 | ns |
| $t_{PZL}$* | | | | | 4.8 | 8.6 | 1 | 10 | |
| $t_{PHZ}$* | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$* | | | | | | | | | |
| $t_{PLH}$ | RCLK | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 6.9 | 9.4 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.9 | 9.4 | 1 | 10.5 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | $C_L$ = 50 pF | | 7.7 | 10.2 | 1 | 11.4 | ns |
| $t_{PHL}$ | | | | | 7.7 | 10.2 | 1 | 11.4 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | $C_L$ = 50 pF | | 7.4 | 10 | 1 | 11.1 | ns |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 8.3 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 8.3 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | OE | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 7.6 | 10.3 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 7.6 | 10.3 | 1 | 11 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHC595 $T_A$ = 25°C MIN | TYP | MAX | SN74AHC595 MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $C_L$ = 15 pF | 135 | 185 | | 115 | | MHz |
| | | | $C_L$ = 50 pF | 95 | 155 | | 85 | | |
| $t_{PLH}$ | RCLK | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 5.4 | 7.4 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.4 | 7.4 | 1 | 8.5 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | $C_L$ = 15 pF | | 6.2 | 8.2 | 1 | 9.4 | ns |
| $t_{PHL}$ | | | | | 6.2 | 8.2 | 1 | 9.4 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | $C_L$ = 15 pF | | 5.9 | 8 | 1 | 9.1 | ns |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 4.8 | 8.6 | 1 | 10 | ns |
| $t_{PZL}$ | | | | | 4.8 | 8.6 | 1 | 10 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |
| $t_{PLH}$ | RCLK | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 6.9 | 9.4 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.9 | 9.4 | 1 | 10.5 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | $C_L$ = 50 pF | | 7.7 | 10.2 | 1 | 11.4 | ns |
| $t_{PHL}$ | | | | | 7.7 | 10.2 | 1 | 11.4 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | $C_L$ = 50 pF | | 7.4 | 10 | 1 | 11.1 | ns |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 8.3 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 8.3 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 7.6 | 10.3 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 7.6 | 10.3 | 1 | 11 | |

## output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC595 $T_A$ = 25°C MIN | MAX | SN74AHC595 MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHC595 MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

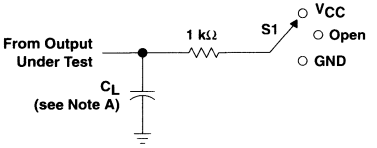
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

PRODUCT PREVIEW

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

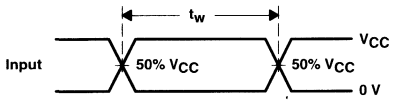
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 87 | pF |

## PARAMETER MEASUREMENT INFORMATION

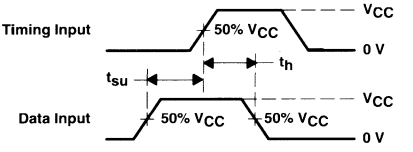



LOAD CIRCUIT

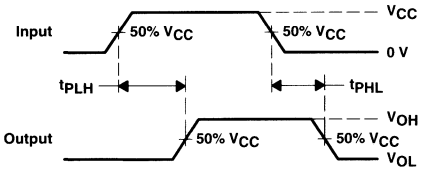
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



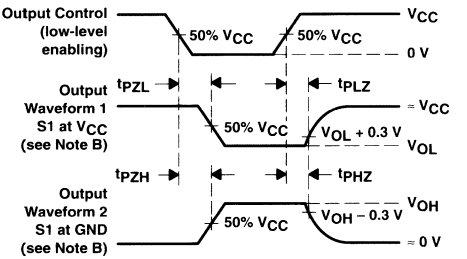

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES



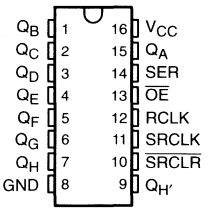

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

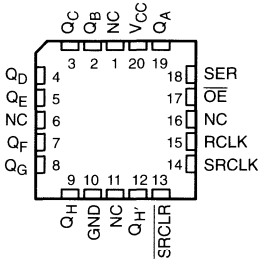
**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **8-Bit Serial-In, Parallel-Out Shift**
- **Shift Register Has Direct Clear**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT595 . . . J OR W PACKAGE**
**SN74AHCT595 . . . D, DB, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT595 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'AHCT595 contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and serial outputs for cascading. When the output-enable ($\overline{OE}$) input is high, the outputs are in the high-impedance state.

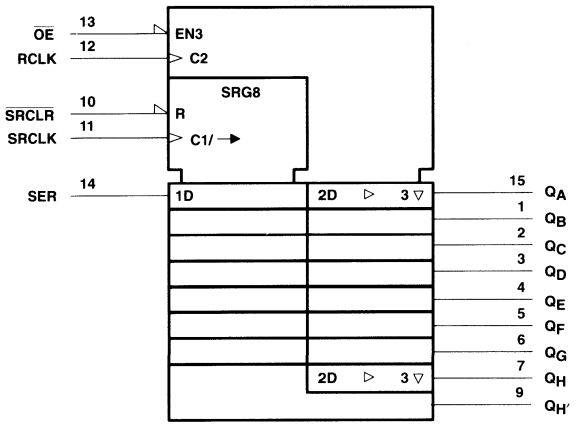
Both the shift register clock (RCLK) and storage register clock (SRCLK) are positive-edge triggered. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

The SN54AHCT595 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT595 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

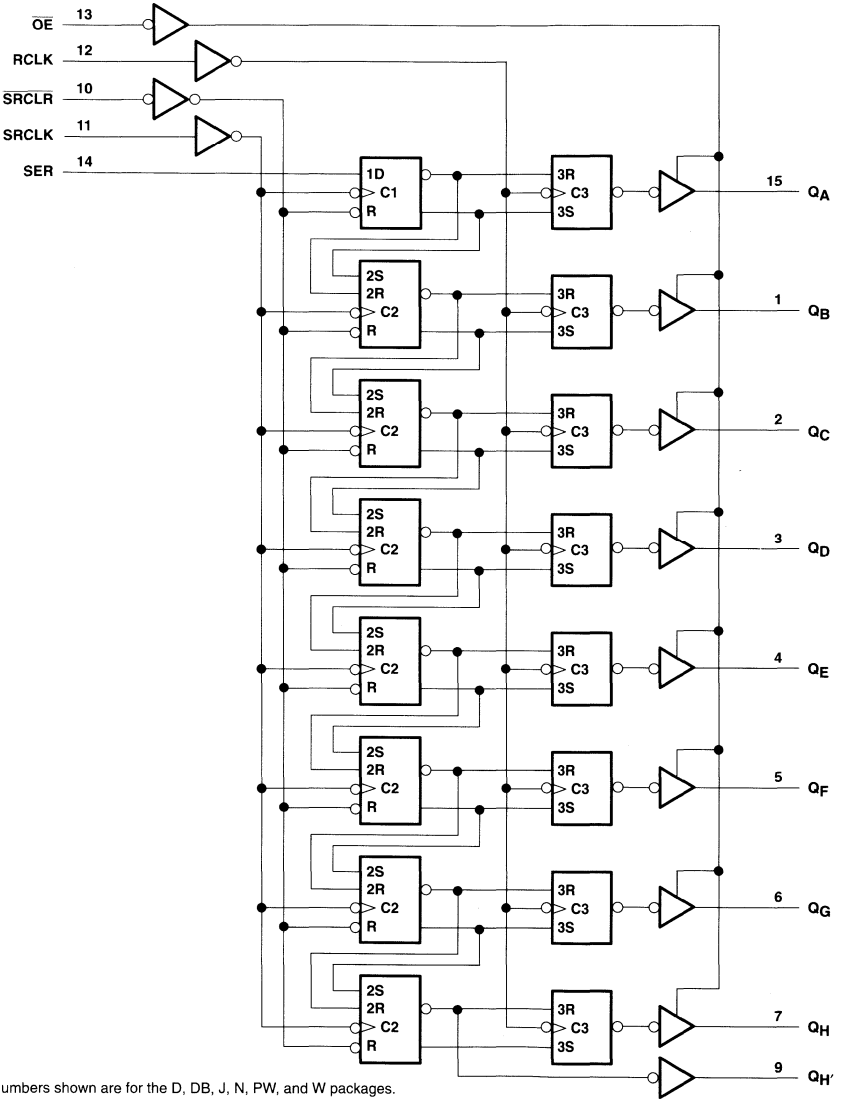
EPIC is a trademark of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

### absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... 113°C/W
DB package ..... 131°C/W
N package ..... 78°C/W
PW package ..... 149°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | SN54AHCT595 | | SN74AHCT595 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT595 | | SN74AHCT595 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54AHCT595 | | SN74AHCT595 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | SRCLK high or low | 5 | | 5 | | 5 | | ns |
| | | RCLK high or low | 5 | | 5 | | 5 | | |
| | | $\overline{SRCLR}$ low | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time | SER before SRCLK↑ | 3 | | 3 | | 3 | | ns |
| | | SRCLK↑ before RCLK↑† | 5 | | 5 | | 5 | | |
| | | $\overline{SRCLR}$ low before RCLK↑ | 5 | | 5 | | 5 | | |
| | | $\overline{SRCLR}$ high (inactive) before SRCLK↑ | 2.5 | | 2.5 | | 2.5 | | |
| $t_h$ | Hold time | SER after SRCLK↑ | 2 | | 2 | | 2 | | ns |
| | | SRCLK↑ after RCLK↑ | 0 | | 0 | | 0 | | |
| | | $\overline{SRCLR}$ low after RCLK↑ | 0 | | 0 | | 0 | | |

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT595 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 135 | 185 | | 115 | | MHz |
| | | | $C_L$ = 50 pF | 95 | 155 | | 85 | | |
| $t_{PLH}$* | RCLK | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 5.4 | 7.4 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5.4 | 7.4 | 1 | 8.5 | |
| $t_{PLH}$* | SRCLK | $Q_{H'}$ | $C_L$ = 15 pF | | 6.2 | 8.2 | 1 | 9.4 | ns |
| $t_{PHL}$* | | | | | 6.2 | 8.2 | 1 | 9.4 | |
| $t_{PHL}$* | $\overline{SRCLR}$ | $Q_{H'}$ | $C_L$ = 15 pF | | 5.9 | 8 | 1 | 9.1 | ns |
| $t_{PZH}$* | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 4.8 | 8.6 | 1 | 10 | ns |
| $t_{PZL}$* | | | | | 4.8 | 8.6 | 1 | 10 | |
| $t_{PHZ}$* | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$* | | | | | | | | | |
| $t_{PLH}$ | RCLK | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 6.9 | 9.4 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.9 | 9.4 | 1 | 10.5 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | $C_L$ = 50 pF | | 7.7 | 10.2 | 1 | 11.4 | ns |
| $t_{PHL}$ | | | | | 7.7 | 10.2 | 1 | 11.4 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | $C_L$ = 50 pF | | 7.4 | 10 | 1 | 11.1 | ns |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 8.3 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 8.3 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 7.6 | 10.3 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 7.6 | 10.3 | 1 | 11 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT595 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | $C_L$ = 15 pF | 135 | 185 | | 115 | | MHz |
| | | | $C_L$ = 50 pF | 95 | 155 | | 85 | | |
| $t_{PLH}$ | RCLK | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 5.4 | 7.4 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.4 | 7.4 | 1 | 8.5 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | $C_L$ = 15 pF | | 6.2 | 8.2 | 1 | 9.4 | ns |
| $t_{PHL}$ | | | | | 6.2 | 8.2 | 1 | 9.4 | |
| $t_{PHL}$ | SRCLR | $Q_{H'}$ | $C_L$ = 15 pF | | 5.9 | 8 | 1 | 9.1 | ns |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 4.8 | 8.6 | 1 | 10 | ns |
| $t_{PZL}$ | | | | | 4.8 | 8.6 | 1 | 10 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | | | | | ns |
| $t_{PLZ}$ | | | | | | | | | |
| $t_{PLH}$ | RCLK | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 6.9 | 9.4 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.9 | 9.4 | 1 | 10.5 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | $C_L$ = 50 pF | | 7.7 | 10.2 | 1 | 11.4 | ns |
| $t_{PHL}$ | | | | | 7.7 | 10.2 | 1 | 11.4 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | $C_L$ = 50 pF | | 7.4 | 10 | 1 | 11.1 | ns |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 8.3 | 10.6 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 8.3 | 10.6 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 7.6 | 10.3 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 7.6 | 10.3 | 1 | 11 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT595 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

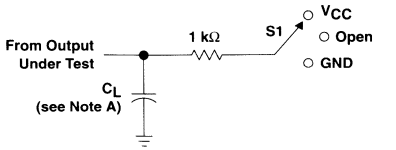
| PARAMETER | | SN74AHCT595 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

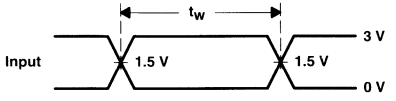
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 87 | pF |

## PARAMETER MEASUREMENT INFORMATION

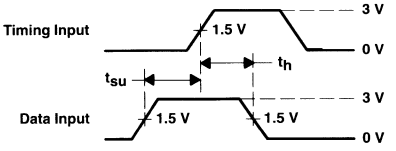



LOAD CIRCUIT

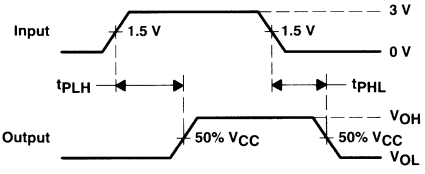
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



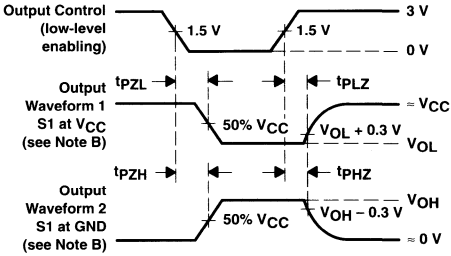

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

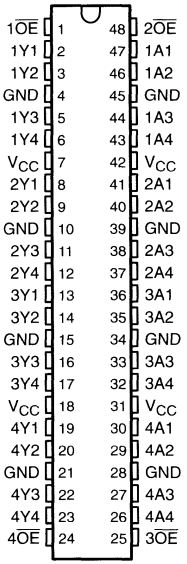
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## Contents

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHC16240 . . . WD PACKAGE**
**SN74AHC16240 . . . DGG, DGV, OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'AHC16240 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide inverting outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The SN54AHC16240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16240 is characterized for operation from –40°C to 85°C.

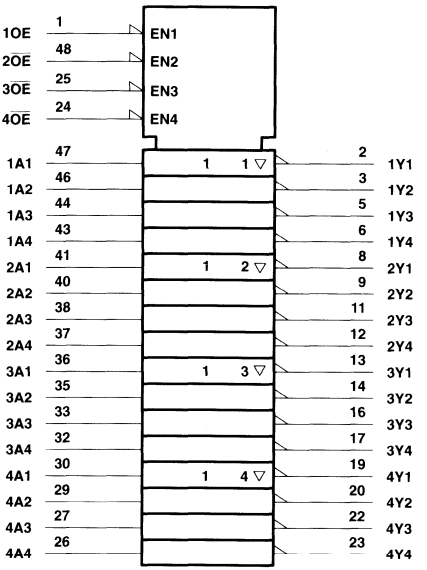
**FUNCTION TABLE**
**(each 4-bit buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

PRODUCT PREVIEW

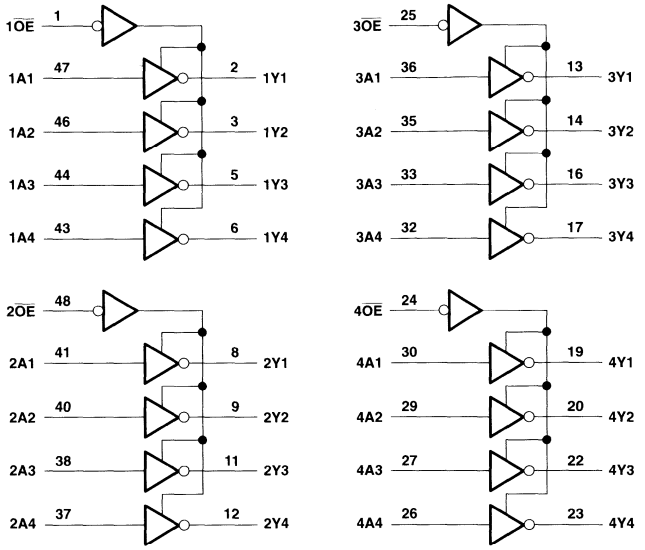
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

### logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through each $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package ..... 89°C/W
DGV package ..... 93°C/W
DL package ..... 94°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

PRODUCT PREVIEW

## recommended operating conditions (see Note 3)

| | | | SN54AHC16240 | | SN74AHC16240 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC16240 | | SN74AHC16240 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | Data inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| | Control inputs | | | | | ±0.1 | | ±1 | | ±1 | |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND, $V_I$ ($\overline{OE}$) = $V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_o$ | | $V_O$ = $V_{CC}$ or GND | 5 V | | 3.5 | | | | | | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16240 | | SN74AHC16240 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5.3 | 7.5 | 1 | 9 | 1 | 9 | ns |
| $t_{PHL}$* | | | | | 5.3 | 7.5 | 1 | 9 | 1 | 9 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6.6 | 10.6 | 1 | 12.5 | 1 | 12.5 | ns |
| $t_{PZL}$* | | | | | 6.6 | 10.6 | 1 | 12.5 | 1 | 12.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7.8 | 11.5 | 1 | 12.5 | 1 | 12.5 | ns |
| $t_{PLZ}$* | | | | | 7.8 | 11.5 | 1 | 12.5 | 1 | 12.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.8 | 11 | 1 | 12.5 | 1 | 12.5 | ns |
| $t_{PHL}$ | | | | | 7.8 | 11 | 1 | 12.5 | 1 | 12.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 9.1 | 14.1 | 1 | 16 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 9.1 | 14.1 | 1 | 16 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 10.3 | 14 | 1 | 16 | 1 | 16 | ns |
| $t_{PLZ}$ | | | | | 10.3 | 14 | 1 | 16 | 1 | 16 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16240 | | SN74AHC16240 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.6 | 5.5 | 1 | 6.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.6 | 5.5 | 1 | 6.5 | 1 | 6.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.7 | 7.3 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PZL}$* | | | | | 4.7 | 7.3 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.2 | 7.2 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PLZ}$* | | | | | 5.2 | 7.2 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.1 | 7.5 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.1 | 7.5 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 6.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.7 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 6.7 | 9.2 | 1 | 10.5 | 1 | 10.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC16240 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

PRODUCT PREVIEW

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHC16240 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.6 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.6 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.6 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

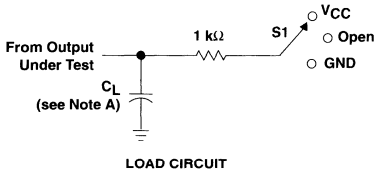
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 10 | pF |

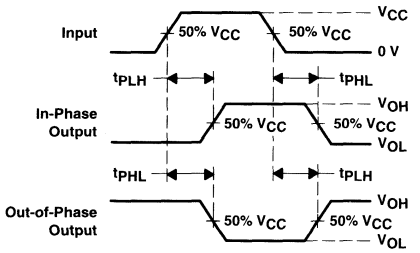


## PARAMETER MEASUREMENT INFORMATION

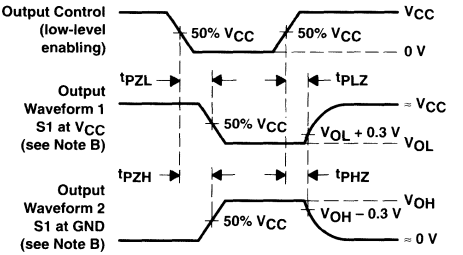



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



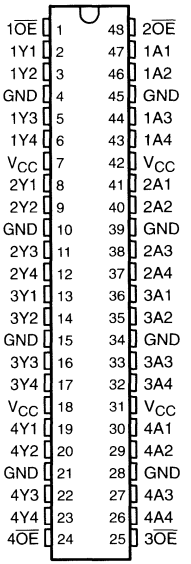

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHCT16240 . . . WD PACKAGE**
**SN74AHCT16240 . . . DGG, DGV, OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'AHCT16240 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide inverting outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The SN54AHCT16240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16240 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each 4-bit buffer)**

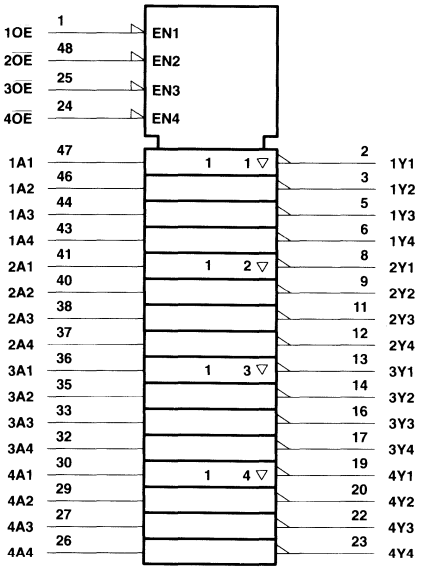
| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

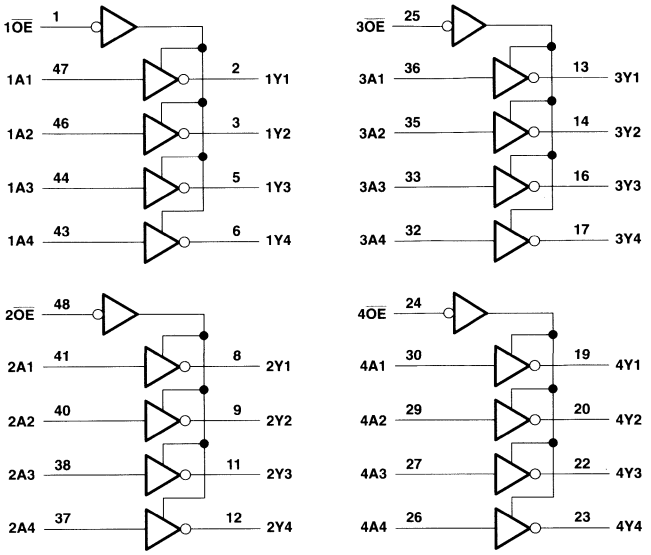
PRODUCT PREVIEW

**logic symbol†**




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through each $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package ..... 89°C/W
DGV package ..... 93°C/W
DL package ..... 94°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

PRODUCT PREVIEW

## recommended operating conditions (see Note 3)

| | | SN54AHCT16240 | | SN74AHCT16240 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT16240 | | SN74AHCT16240 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 3 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHCT16240 | | SN74AHCT16240 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5.4 | 7.4 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5.4 | 7.4 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7.7 | 10.4 | 1 | 12 | 1 | 12 | ns |
| $t_{PZL}$* | | | | | 7.7 | 10.4 | 1 | 12 | 1 | 12 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 8.3 | 10.4 | 1 | 12 | 1 | 12 | ns |
| $t_{PLZ}$* | | | | | 8.3 | 10.4 | 1 | 12 | 1 | 12 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.9 | 8.4 | 1 | 9.5 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.9 | 8.4 | 1 | 9.5 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.2 | 11.4 | 1 | 13 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 8.2 | 11.4 | 1 | 13 | 1 | 13 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.8 | 11.4 | 1 | 13 | 1 | 13 | ns |
| $t_{PLZ}$ | | | | | 8.8 | 11.4 | 1 | 13 | 1 | 13 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT16240 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHCT16240 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.6 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.6 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.1 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

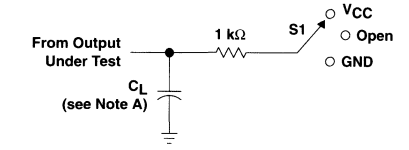
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 10 | pF |

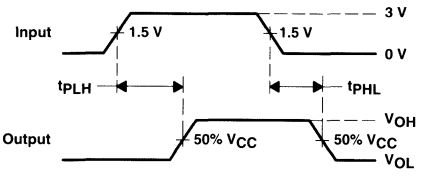
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION

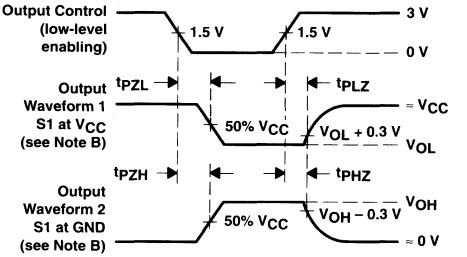



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



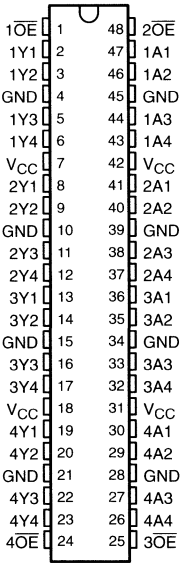

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHC16244 . . . WD PACKAGE**
**SN74AHC16244 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'AHC16244 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The SN54AHC16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16244 is characterized for operation from –40°C to 85°C.

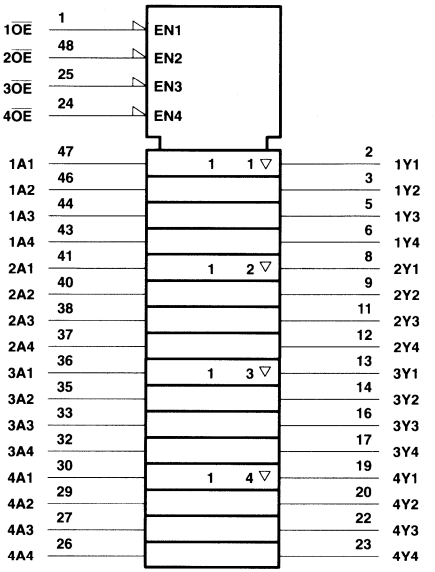
**FUNCTION TABLE**
**(each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

PRODUCT PREVIEW

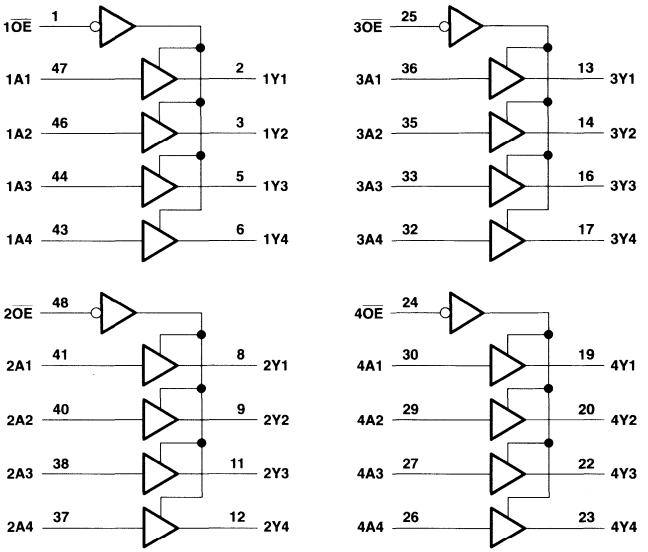
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

**logic symbol†**




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through each $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package ..... 89°C/W
DL package ..... 94°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

PRODUCT PREVIEW

## recommended operating conditions (see Note 3)

| | | | SN54AHC16244 | | SN74AHC16244 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC16244 | | SN74AHC16244 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | Data inputs | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| | Control inputs | | | | | ±0.1 | | ±1 | | ±1 | |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND, $V_I$ ($\overline{OE}$) = $V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| $C_o$ | | $V_O$ = $V_{CC}$ or GND | 5 V | | 3.5 | | | | | | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16244 | | SN74AHC16244 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5.8 | 8.4 | 1 | 10 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 5.8 | 8.4 | 1 | 10 | 1 | 10 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6.6 | 10.6 | 1 | 12.5 | 1 | 12.5 | ns |
| $t_{PZL}$* | | | | | 6.6 | 10.6 | 1 | 12.5 | 1 | 12.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 9.7 | 1 | 11 | 1 | 11 | ns |
| $t_{PLZ}$* | | | | | 5 | 9.7 | 1 | 11 | 1 | 11 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 8.3 | 11.9 | 1 | 13.5 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 8.3 | 11.9 | 1 | 13.5 | 1 | 13.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 9.1 | 14.1 | 1 | 16 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 9.1 | 14.1 | 1 | 16 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 10.3 | 14 | 1 | 16 | 1 | 16 | ns |
| $t_{PLZ}$ | | | | | 10.3 | 14 | 1 | 16 | 1 | 16 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16244 | | SN74AHC16244 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.9 | 5.5 | 1 | 6.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.9 | 5.5 | 1 | 6.5 | 1 | 6.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.7 | 7.3 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PZL}$* | | | | | 4.7 | 7.3 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 7.2 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PLZ}$* | | | | | 5 | 7.2 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.4 | 7.5 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.4 | 7.5 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 6.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.7 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 6.7 | 9.2 | 1 | 10.5 | 1 | 10.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC16244 | | UNIT |
|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | |
| | | | MIN | MAX | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | | 1.5 | ns |
| | | 5 V ± 0.5 V | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

PRODUCT PREVIEW

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHC16244 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.5 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.2 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.8 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

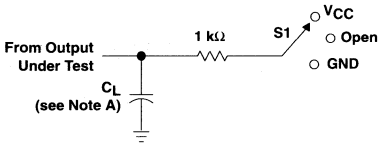
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 8.6 | pF |

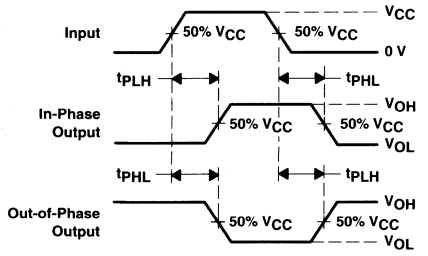
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION

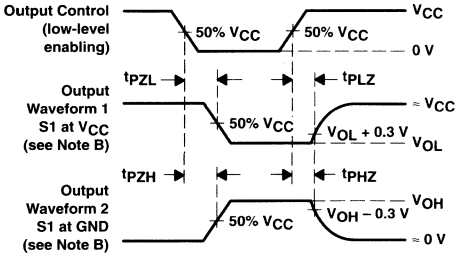



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



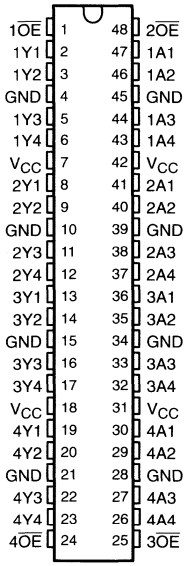

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHCT16244 . . . WD PACKAGE**
**SN74AHCT16244 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'AHCT16244 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The SN54AHCT16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16244 is characterized for operation from –40°C to 85°C.

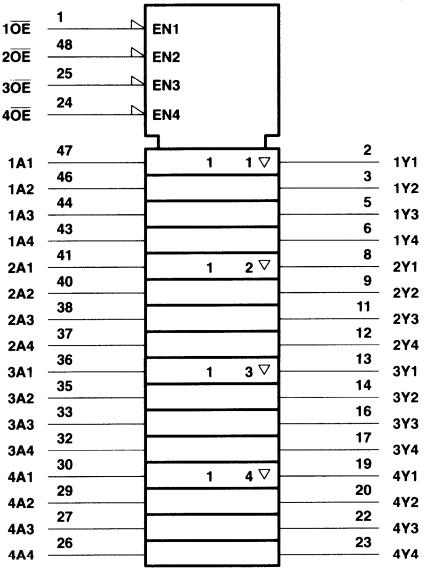
**FUNCTION TABLE**
**(each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

PRODUCT PREVIEW

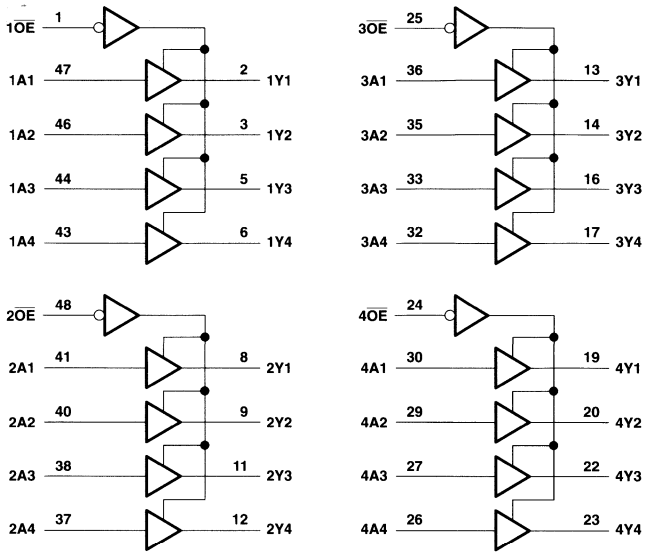
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$ (see Note 1) | –0.5 V to 7 V |
| Output voltage range, $V_O$ (see Note 1) | –0.5 V to $V_{CC}$ + 0.5 V |
| Input clamp current, $I_{IK}$ ($V_I$ < 0) | –20 mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) | ±20 mA |
| Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) | ±25 mA |
| Continuous current through each $V_{CC}$ or GND | ±75 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package | 89°C/W |
| DL package | 94°C/W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

PRODUCT PREVIEW

## recommended operating conditions (see Note 3)

| | | SN54AHCT16244 | | SN74AHCT16244 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT16244 | | SN74AHCT16244 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 3 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHCT16244 | | SN74AHCT16244 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5.4 | 7.4 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5.4 | 7.4 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7.7 | 10.4 | 1 | 12 | 1 | 12 | ns |
| $t_{PZL}$* | | | | | 7.7 | 10.4 | 1 | 12 | 1 | 12 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 9.4 | 1 | 10 | 1 | 10 | ns |
| $t_{PLZ}$* | | | | | 5 | 9.4 | 1 | 10 | 1 | 10 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.9 | 8.4 | 1 | 9.5 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.9 | 8.4 | 1 | 9.5 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.2 | 11.4 | 1 | 13 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 8.2 | 11.4 | 1 | 13 | 1 | 13 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.8 | 11.4 | 1 | 13 | 1 | 13 | ns |
| $t_{PLZ}$ | | | | | 8.8 | 11.4 | 1 | 13 | 1 | 13 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT16244 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHCT16244 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.7 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.7 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.1 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

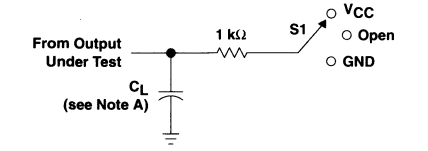
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 8.2 | pF |

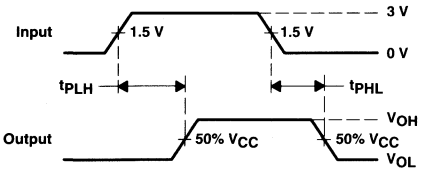
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION

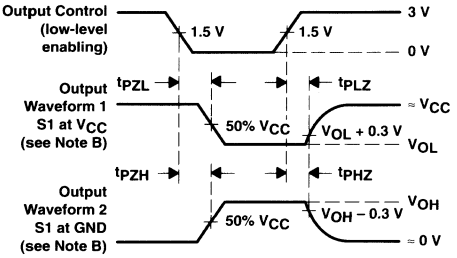



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



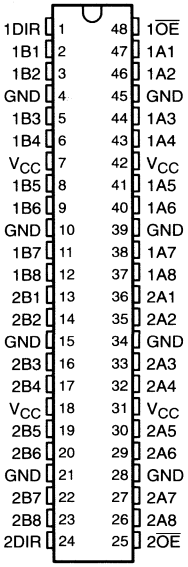

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHC16245 . . . WD PACKAGE**
**SN74AHC16245 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'AHC16245 are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The SN54AHC16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16245 is characterized for operation from –40°C to 85°C.

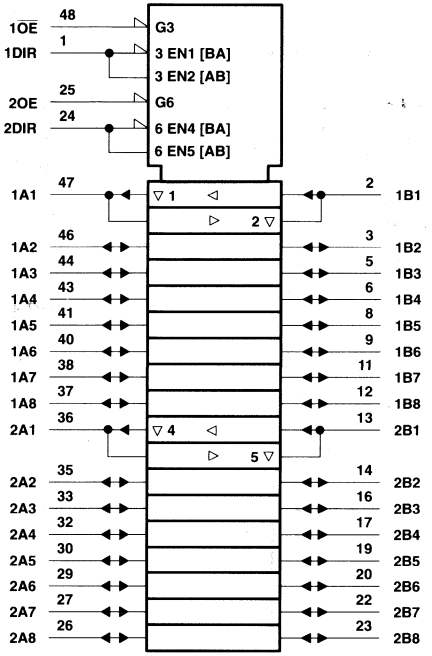
**FUNCTION TABLE**
**(each 8-bit section)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

PRODUCT PREVIEW

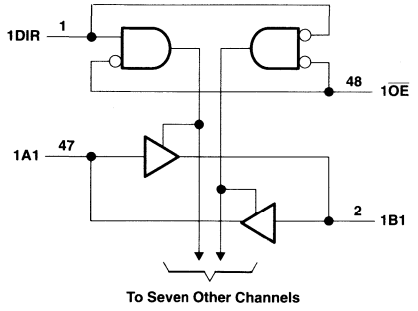
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

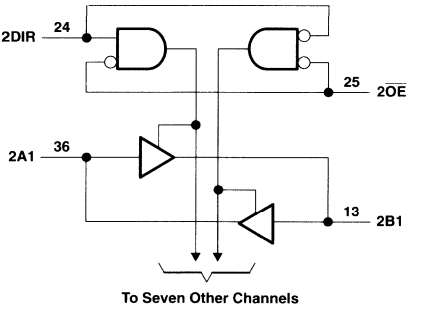
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 89°C/W
DL package . . . . . 94°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | | SN54AHC16245 | | SN74AHC16245 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | µA |
| | | $V_{CC}$ = 3.3 ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | µA |
| | | $V_{CC}$ = 3.3 ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC16245 | | SN74AHC16245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | A or B inputs | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| | $\overline{OE}$ or DIR | | | | | ±0.1 | | ±1 | | ±1 | |
| $I_{OZ}$† | | $V_O = V_{CC}$ or GND, $V_I$ ($\overline{OE}$) = $V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $\overline{OE}$ or DIR | $V_I = V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_{io}$ | A or B inputs | $V_I = V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

† The parameter $I_{OZ}$ includes the input leakage current.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16245 | | SN74AHC16245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A or B | B or A | $C_L$ = 15 pF | | 5.8 | 8.4 | 1 | 10 | 1 | 10 | ns |
| $t_{PHL}$* | | | | | 5.8 | 8.4 | 1 | 10 | 1 | 10 | |
| $t_{PZH}$* | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 8.5 | 13.2 | 1 | 15.5 | 1 | 15.5 | ns |
| $t_{PZL}$* | | | | | 8.5 | 13.2 | 1 | 15.5 | 1 | 15.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 8.9 | 12.5 | 1 | 15.5 | 1 | 15.5 | ns |
| $t_{PLZ}$* | | | | | 8.9 | 12.5 | 1 | 15.5 | 1 | 15.5 | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 50 pF | | 8.3 | 11.9 | 1 | 13.5 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 8.3 | 11.9 | 1 | 13.5 | 1 | 13.5 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 11 | 16.7 | 1 | 19 | 1 | 19 | ns |
| $t_{PZL}$ | | | | | 11 | 16.7 | 1 | 19 | 1 | 19 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 11.5 | 15.8 | 1 | 18 | 1 | 18 | ns |
| $t_{PLZ}$ | | | | | 11.5 | 15.8 | 1 | 18 | 1 | 18 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16245 | | SN74AHC16245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A or B | B or A | $C_L$ = 15 pF | | 4 | 5.5 | 1 | 6.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 4 | 5.5 | 1 | 6.5 | 1 | 6.5 | |
| $t_{PZH}$* | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 5.8 | 8.5 | 1 | 10 | 1 | 10 | ns |
| $t_{PZL}$* | | | | | 5.8 | 8.5 | 1 | 10 | 1 | 10 | |
| $t_{PHZ}$* | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 5.6 | 7.8 | 1 | 9.2 | 1 | 9.2 | ns |
| $t_{PLZ}$* | | | | | 5.6 | 7.8 | 1 | 9.2 | 1 | 9.2 | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 50 pF | | 5.5 | 7.5 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.5 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 7.3 | 10.6 | 1 | 12 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.3 | 10.6 | 1 | 12 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 7 | 9.7 | 1 | 11 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 7 | 9.7 | 1 | 11 | 1 | 11 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC16245 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX |
| | | | MIN | MAX | | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHC16245 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.9 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.9 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.3 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

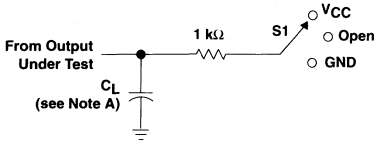
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 14 | pF |

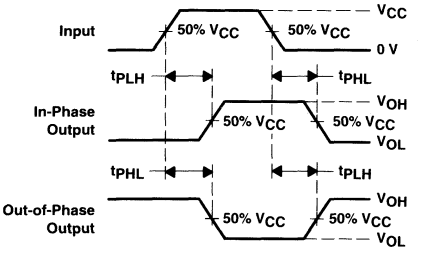
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION

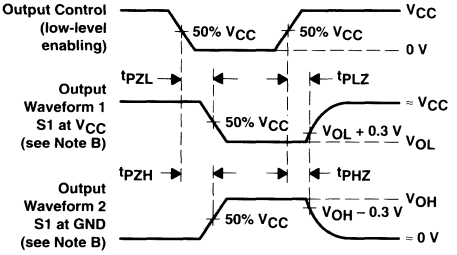



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



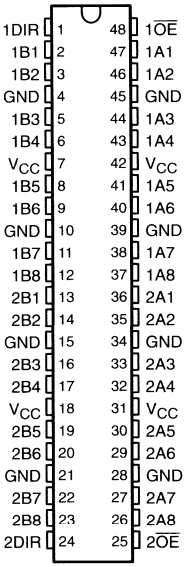

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHCT16245 . . . WD PACKAGE**
**SN74AHCT16245 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'AHCT16245 are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The SN54AHCT16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16245 is characterized for operation from –40°C to 85°C.

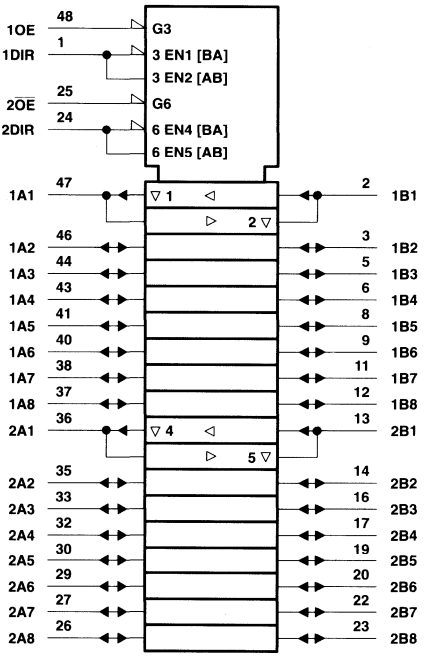
**FUNCTION TABLE**
***(each 8-bit section)***

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

PRODUCT PREVIEW

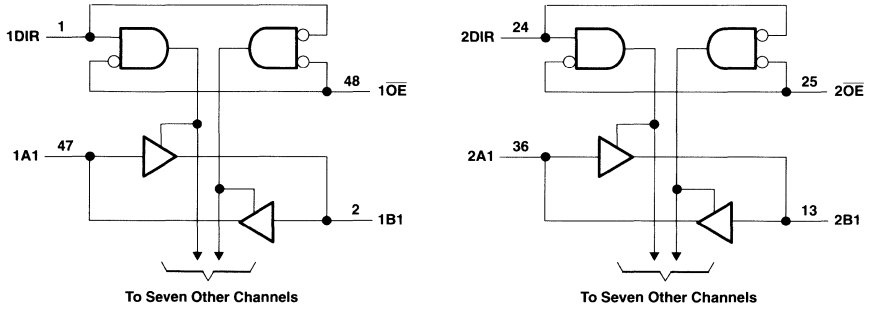
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through each $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package ..... 89°C/W
DL package ..... 94°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | SN54AHCT16245 | | SN74AHCT16245 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_{IO}$ | Input/output voltage, A or B pins | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT16245 | | SN74AHCT16245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$‡ | A or B inputs | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $\overline{OE}$ or DIR | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$§ | | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $\overline{OE}$ or DIR | $V_I$ = $V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_{io}$ | A or B inputs | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
§ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHCT16245 | | SN74AHCT16245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A or B | B or A | $C_L$ = 15 pF | | 4.5 | 7.7 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 4.5 | 7.7 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PZH}$* | OE | A or B | $C_L$ = 15 pF | | 8.9 | 13.8 | 1 | 15 | 1 | 15 | ns |
| $t_{PZL}$* | | | | | 8.9 | 13.8 | 1 | 15 | 1 | 15 | |
| $t_{PHZ}$* | OE | A or B | $C_L$ = 15 pF | | 9.2 | 14.4 | 1 | 15.5 | 1 | 15.5 | ns |
| $t_{PLZ}$* | | | | | 9.2 | 14.4 | 1 | 15.5 | 1 | 15.5 | |
| $t_{PLH}$ | A or B | B or A | $C_L$ = 50 pF | | 5.3 | 8.7 | 1 | 9.5 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 8.7 | 1 | 9.5 | 1 | 9.5 | |
| $t_{PZH}$ | OE | A or B | $C_L$ = 50 pF | | 9.7 | 14.8 | 1 | 16 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 9.7 | 14.8 | 1 | 16 | 1 | 16 | |
| $t_{PHZ}$ | OE | A or B | $C_L$ = 50 pF | | 10 | 15.4 | 1 | 16.5 | 1 | 16.5 | ns |
| $t_{PLZ}$ | | | | | 10 | 15.4 | 1 | 16.5 | 1 | 16.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT16245 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHCT16245 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

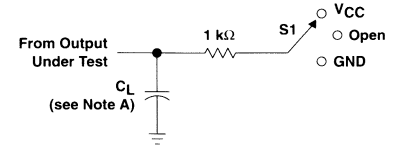
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 13 | pF |

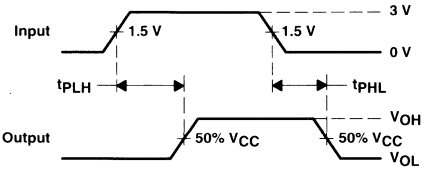
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION

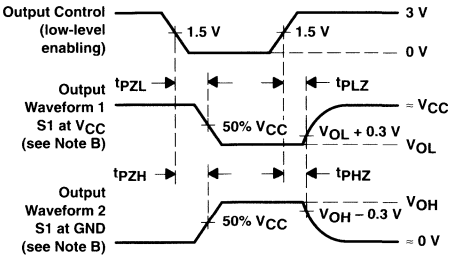



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

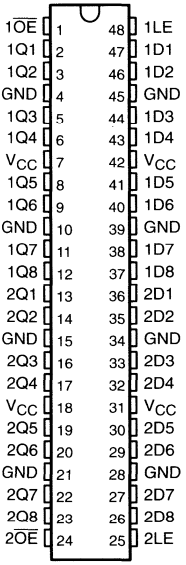
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHC16373 . . . WD PACKAGE**
**SN74AHC16373 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'AHC16373 are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHC16373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16373 is characterized for operation from –40°C to 85°C.

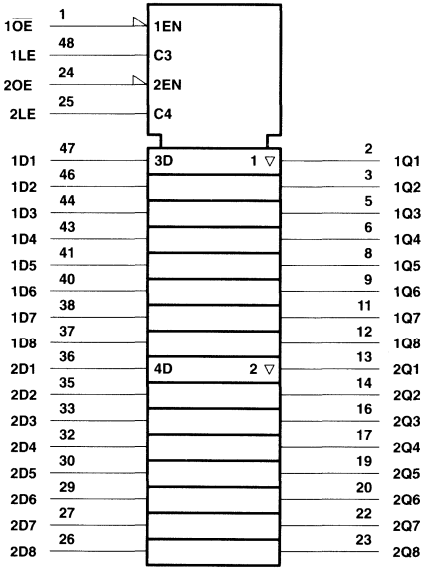
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

**FUNCTION TABLE**
**(each latch)**

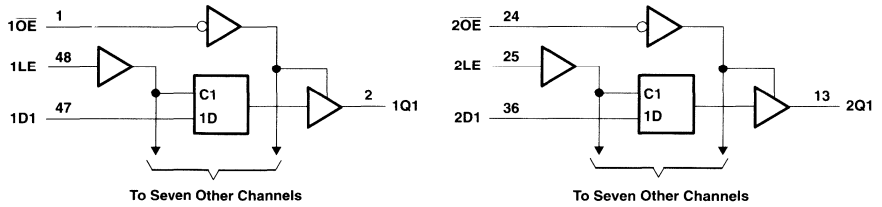
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 89°C/W
DL package . . . . . 94°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | | SN54AHC16373 | | SN74AHC16373 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC16373 | | SN74AHC16373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND, $V_I = V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 6 | | | | | | pF |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHC16373 | | SN74AHC16373 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 4 | | 4 | | 4 | | ns |
| $t_h$ | Hold time, data after LE↓ | 1 | | 1 | | 1 | | ns |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHC16373 | | SN74AHC16373 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 4 | | 4 | | 4 | | ns |
| $t_h$ | Hold time, data after LE↓ | 1 | | 1 | | 1 | | ns |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16373 | | SN74AHC16373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | D | Q | $C_L$ = 15 pF | | 7.3 | 11.4 | 1 | 13.5 | 1 | 13.5 | ns |
| $t_{PHL}$* | | | | | 7.3 | 11.4 | 1 | 13.5 | 1 | 13.5 | |
| $t_{PLH}$* | LE | Q | $C_L$ = 15 pF | | 7 | 11 | 1 | 13 | 1 | 13 | ns |
| $t_{PHL}$* | | | | | 7 | 11 | 1 | 13 | 1 | 13 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.3 | 11.4 | 1 | 13.5 | 1 | 13.5 | ns |
| $t_{PZL}$* | | | | | 7.3 | 11.4 | 1 | 13.5 | 1 | 13.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7 | 10 | 1 | 12 | 1 | 12 | ns |
| $t_{PLZ}$* | | | | | 7 | 10 | 1 | 12 | 1 | 12 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 9.8 | 14.9 | 1 | 17 | 1 | 17 | ns |
| $t_{PHL}$ | | | | | 9.8 | 14.9 | 1 | 17 | 1 | 17 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 9.5 | 14.5 | 1 | 16.5 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | | 9.5 | 14.5 | 1 | 16.5 | 1 | 16.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.8 | 14.9 | 1 | 17 | 1 | 17 | ns |
| $t_{PZL}$ | | | | | 9.8 | 14.9 | 1 | 17 | 1 | 17 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.5 | 13.2 | 1 | 15 | 1 | 15 | ns |
| $t_{PLZ}$ | | | | | 9.5 | 13.2 | 1 | 15 | 1 | 15 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16373 | | SN74AHC16373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | D | Q | $C_L$ = 15 pF | | 5 | 7.2 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5 | 7.2 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PLH}$* | LE | Q | $C_L$ = 15 pF | | 4.9 | 7.2 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 4.9 | 7.2 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.5 | 8.1 | 1 | 9.5 | 1 | 9.5 | ns |
| $t_{PZL}$* | | | | | 5.5 | 8.1 | 1 | 9.5 | 1 | 9.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5 | 7.2 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PLZ}$* | | | | | 5 | 7.2 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 6.5 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.5 | 9.2 | 1 | 10.5 | 1 | 10.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 6.4 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 9.2 | 1 | 10.5 | 1 | 10.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7 | 10.1 | 1 | 11.5 | 1 | 11.5 | ns |
| $t_{PZL}$ | | | | | 7 | 10.1 | 1 | 11.5 | 1 | 11.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.5 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 6.5 | 9.2 | 1 | 10.5 | 1 | 10.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC16373 $T_A$ = 25°C MIN | SN74AHC16373 $T_A$ = 25°C MAX | SN74AHC16373 MIN | SN74AHC16373 MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | | | 1.5 | 1.5 | ns |
| | | 5 V ± 0.5 V | | | 1 | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHC16373 MIN | SN74AHC16373 TYP | SN74AHC16373 MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.1 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

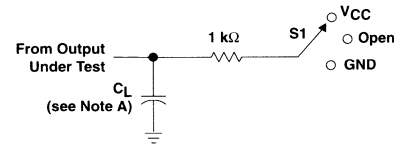
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 18 | pF |

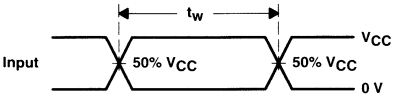
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION

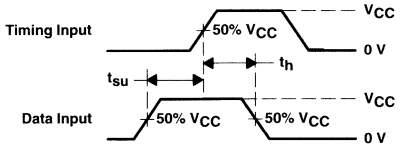



LOAD CIRCUIT

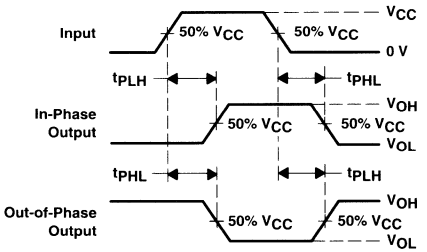
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



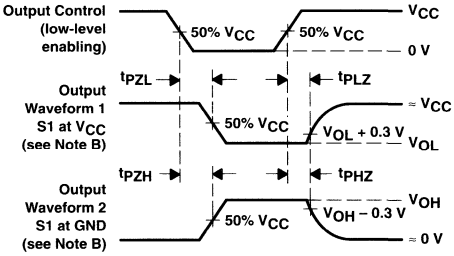

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

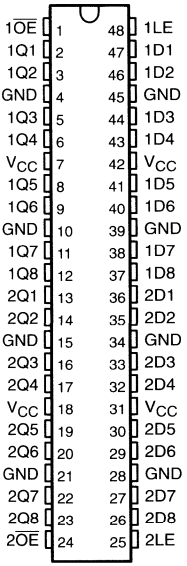
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHCT16373 . . . WD PACKAGE**
**SN74AHCT16373 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'AHCT16373 are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHCT16373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16373 is characterized for operation from –40°C to 85°C.

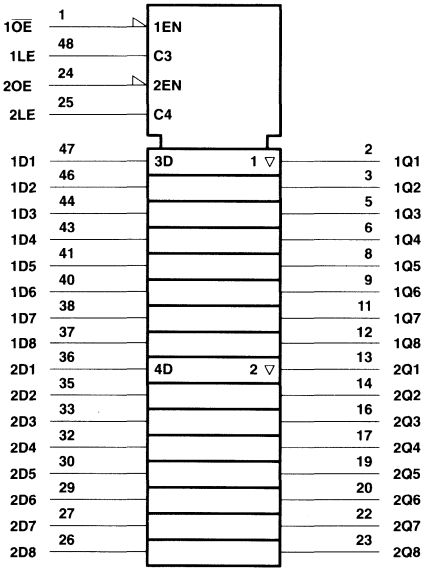
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

**FUNCTION TABLE**
**(each latch)**

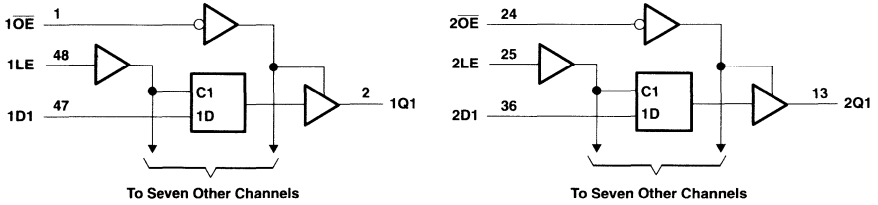
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through each $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package ..... 89°C/W
DL package ..... 94°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | SN54AHCT16373 | | SN74AHCT16373 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_{IO}$ | Input/output voltage, A or B pins | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT16373 | | SN74AHCT16373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | µA |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | µA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 6 | | | | | | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHCT16373 | | SN74AHCT16373 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 6.5 | | 6.5 | | 6.5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 1.5 | | 1.5 | | 1.5 | | ns |
| $t_h$ | Hold time, data after LE↓ | 3.5 | | 3.5 | | 3.5 | | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHCT16373 | | SN74AHCT16373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | D | Q | $C_L$ = 15 pF | | 5.1 | 8.5 | 1 | 9.5 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.1 | 8.5 | 1 | 9.5 | 1 | 9.5 | |
| $t_{PLH}$* | LE | Q | $C_L$ = 15 pF | | 7.7 | 12.3 | 1 | 13.5 | 1 | 13.5 | ns |
| $t_{PHL}$* | | | | | 7.7 | 12.3 | 1 | 13.5 | 1 | 13.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 6.3 | 10.9 | 1 | 12.5 | 1 | 12.5 | ns |
| $t_{PZL}$* | | | | | 6.3 | 10.9 | 1 | 12.5 | 1 | 12.5 | |
| $t_{PHZ}$* | OE | Q | $C_L$ = 15 pF | | 6 | 10.2 | 1 | 11 | 1 | 11 | ns |
| $t_{PLZ}$* | | | | | 6 | 10.2 | 1 | 11 | 1 | 11 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 5.9 | 9.5 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5.9 | 9.5 | 1 | 10.5 | 1 | 10.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 8.5 | 13.3 | 1 | 14.5 | 1 | 14.5 | ns |
| $t_{PHL}$ | | | | | 8.5 | 13.3 | 1 | 14.5 | 1 | 14.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7.1 | 11.9 | 1 | 13.5 | 1 | 13.5 | ns |
| $t_{PZL}$ | | | | | 7.1 | 11.9 | 1 | 13.5 | 1 | 13.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.8 | 11.2 | 1 | 12 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 6.8 | 11.2 | 1 | 12 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT16373 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHCT16373 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | 1.2 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | –1.2 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.1 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

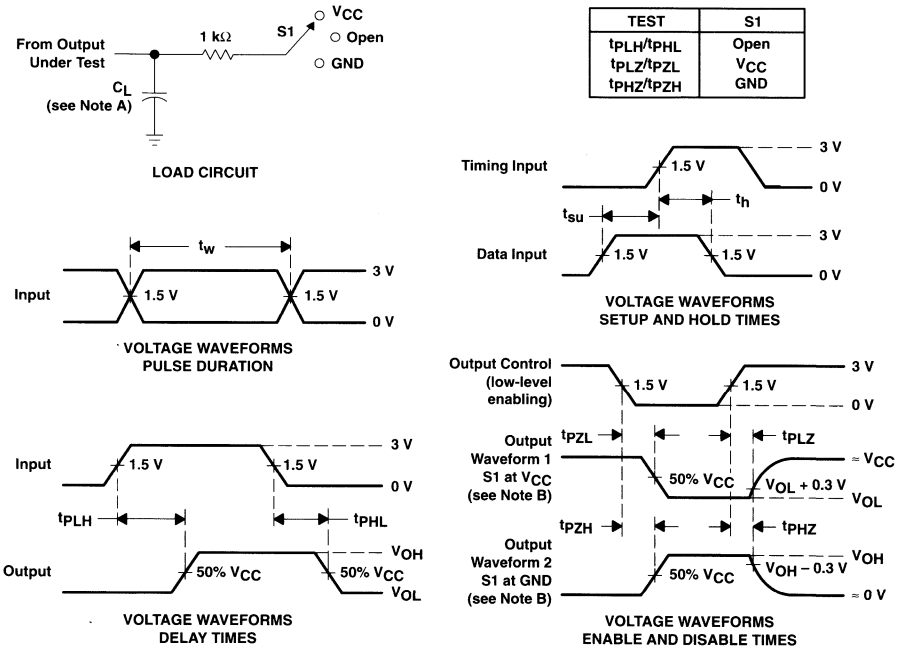
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

PRODUCT PREVIEW

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 17 | pF |

## PARAMETER MEASUREMENT INFORMATION



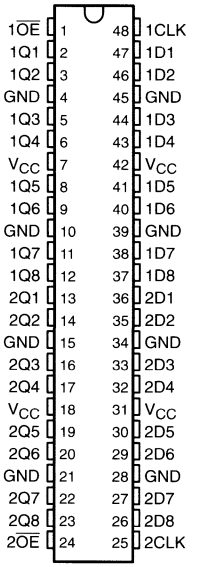

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V $V_{CC}$**
- **3-State Outputs Drive Bus Lines Directly**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHC16374 . . . WD PACKAGE**
**SN74AHC16374 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'AHC16374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHC16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16374 is characterized for operation from –40°C to 85°C.

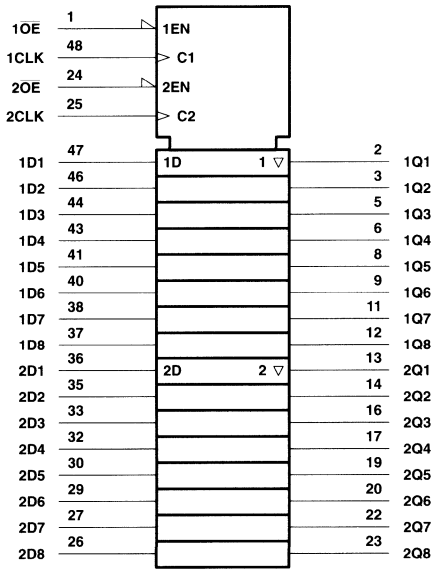
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

**FUNCTION TABLE**
**(each flip-flop)**

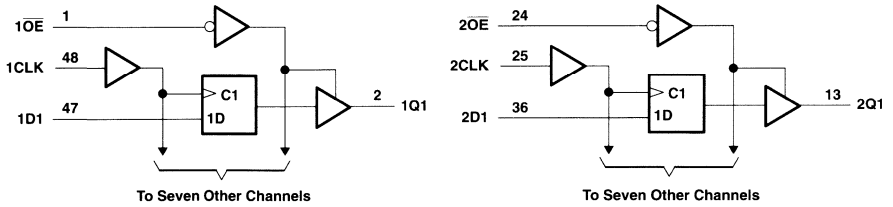
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




PRODUCT PREVIEW

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) ..... ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ..... ±25 mA
Continuous current through each $V_{CC}$ or GND ..... ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package ..... 89°C/W
DL package ..... 94°C/W
Storage temperature range, $T_{stg}$ ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | | SN54AHC16374 | | SN74AHC16374 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC16374 | | SN74AHC16374 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 6 | | | | | | pF |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHC16374 | | SN74AHC16374 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 5 | | 5.5 | | 5.5 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 4.5 | | 4 | | 4 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 2 | | 2 | | 2 | | ns |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHC16374 | | SN74AHC16374 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 3 | | 3 | | 3 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 2 | | 2 | | 2 | | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16374 | | SN74AHC16374 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 80 | 130 | | 70 | | 70 | | MHz |
| | | | $C_L$ = 50 pF | 55 | 85 | | 50 | | 50 | | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 8.1 | 12.7 | 1 | 15 | 1 | 15 | ns |
| $t_{PHL}$* | | | | | 8.1 | 12.7 | 1 | 15 | 1 | 15 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.1 | 11 | 1 | 13 | 1 | 13 | ns |
| $t_{PZL}$* | | | | | 7.1 | 11 | 1 | 13 | 1 | 13 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.5 | 10.5 | 1 | 12.5 | 1 | 12.5 | ns |
| $t_{PLZ}$* | | | | | 7.5 | 10.5 | 1 | 12.5 | 1 | 12.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 10.6 | 16.2 | 1 | 18.5 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.6 | 16.2 | 1 | 18.5 | 1 | 18.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.6 | 14.5 | 1 | 16.5 | 1 | 16.5 | ns |
| $t_{PZL}$ | | | | | 9.6 | 14.5 | 1 | 16.5 | 1 | 16.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 10.2 | 14 | 1 | 16 | 1 | 16 | ns |
| $t_{PLZ}$ | | | | | 10.2 | 14 | 1 | 16 | 1 | 16 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16374 | | SN74AHC16374 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 130 | 185 | | 110 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 120 | | 75 | | 75 | | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 5.4 | 8.1 | 1 | 9.5 | 1 | 9.5 | ns |
| $t_{PHL}$* | | | | | 5.4 | 8.1 | 1 | 9.5 | 1 | 9.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.1 | 7.6 | 1 | 9 | 1 | 9 | ns |
| $t_{PZL}$* | | | | | 5.1 | 7.6 | 1 | 9 | 1 | 9 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | 1 | 8 | ns |
| $t_{PLZ}$* | | | | | 4.6 | 6.8 | 1 | 8 | 1 | 8 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.9 | 10.1 | 1 | 11.5 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.9 | 10.1 | 1 | 11.5 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.6 | 9.6 | 1 | 11 | 1 | 11 | ns |
| $t_{PZL}$ | | | | | 6.6 | 9.6 | 1 | 11 | 1 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | 1 | 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHC16374 | | UNIT |
|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | MIN MAX | |
| | | | MIN MAX | | |
| $t_{sk(o)}$ | Output skew | 3.3 V ± 0.3 V | 1.5 | 1.5 | ns |
| | | 5 V ± 0.5 V | 1 | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHC16374 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.5 | 1 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.5 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

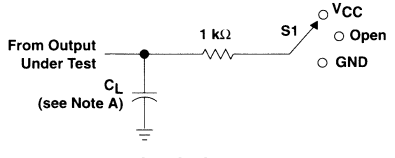
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 32 | pF |

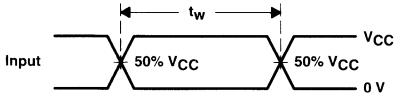
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION

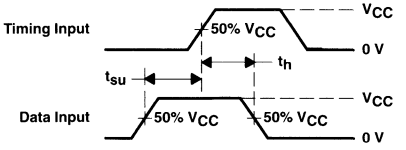



LOAD CIRCUIT

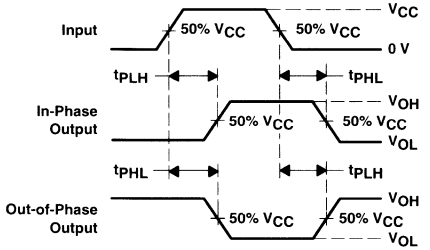
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



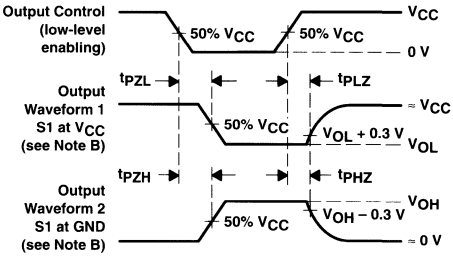

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

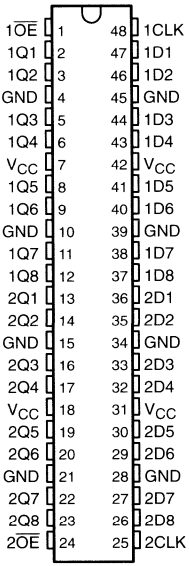
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHCT16374 . . . WD PACKAGE**
**SN74AHCT16374 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'AHCT16374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHCT16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16374 is characterized for operation from –40°C to 85°C.

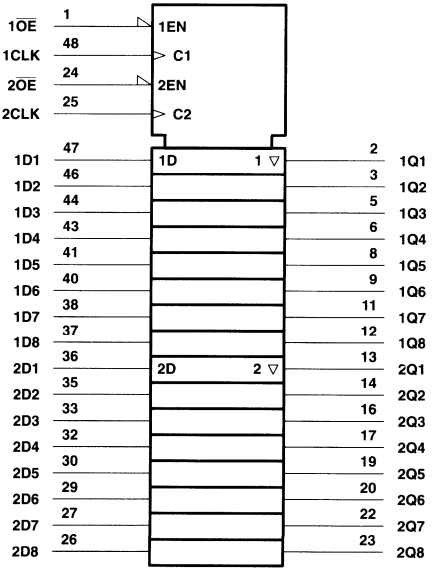
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

**FUNCTION TABLE**
**(each flip-flop)**

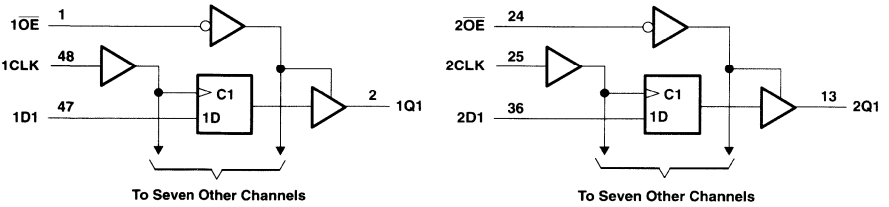
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 89°C/W
DL package . . . . . 94°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | SN54AHCT16374 | | SN74AHCT16374 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_{IO}$ | Input/output voltage, A or B pins | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT16374 | | SN74AHCT16374 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND, $V_I$ = $V_{IH}$ or $V_{IL}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | µA |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | µA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 6 | | | | | | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHCT16374 | | SN74AHCT16374 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 6.5 | | 6.5 | | 6.5 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 2.5 | | 2.5 | | 2.5 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 2.5 | | 2.5 | | 2.5 | | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHCT16374 | | SN74AHCT16374 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF* | 90 | 140 | | 80 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 130 | | 75 | | 75 | | |
| $t_{PLH}$* | CLK | Q | $C_L$ = 15 pF | | 5.6 | 9.4 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PHL}$* | | | | | 5.6 | 9.4 | 1 | 10.5 | 1 | 10.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 6.5 | 10.2 | 1 | 11.5 | 1 | 11.5 | ns |
| $t_{PZL}$* | | | | | 6.5 | 10.2 | 1 | 11.5 | 1 | 11.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 6.2 | 10.2 | 1 | 11 | 1 | 11 | ns |
| $t_{PLZ}$* | | | | | 6.2 | 10.2 | 1 | 11 | 1 | 11 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.4 | 10.4 | 1 | 11.5 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 10.4 | 1 | 11.5 | 1 | 11.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7.3 | 11.2 | 1 | 12.5 | 1 | 12.5 | ns |
| $t_{PZL}$ | | | | | 7.3 | 11.2 | 1 | 12.5 | 1 | 12.5 | |
| $t_{PHZ}$ | OE | Q | $C_L$ = 50 pF | | 7 | 11.2 | 1 | 12 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 7 | 11.2 | 1 | 12 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT16374 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

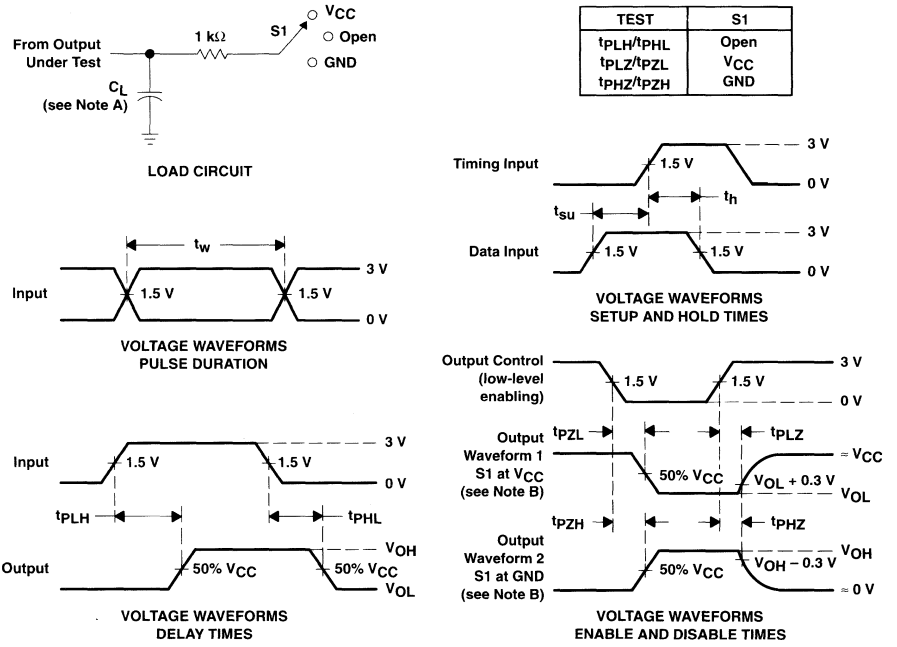
| PARAMETER | | SN74AHCT16374 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | 1.2 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | –1.2 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 3.8 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 27 | pF |

## PARAMETER MEASUREMENT INFORMATION



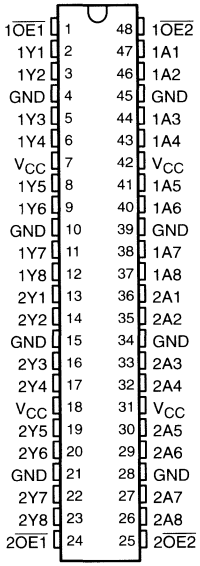

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHC16540 . . . WD PACKAGE**
**SN74AHC16540 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

These 16-bit buffers and bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

The SN54AHC16540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16540 is characterized for operation from –40°C to 85°C.

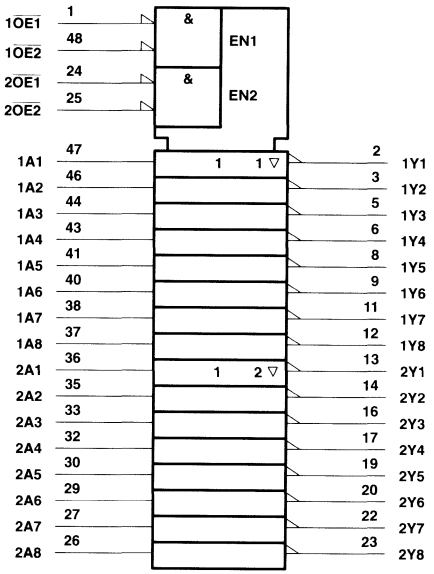
**FUNCTION TABLE**
**(each 8-bit section)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

PRODUCT PREVIEW

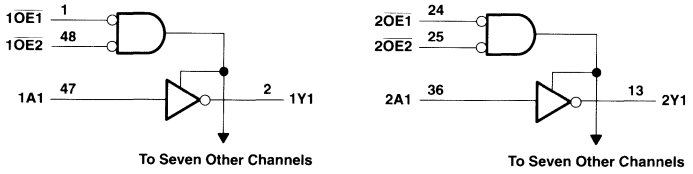
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 89°C/W
DL package . . . . . 94°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | | SN54AHC16540 | | SN74AHC16540 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC16540 | | SN74AHC16540 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | Data inputs | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| | Control inputs | | | | | ±0.1 | | ±1 | | ±1 | |
| $I_{OZ}$ | | $V_O = V_{CC}$ or GND, $V_I$ ($\overline{OE}$) = $V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| $C_o$ | | $V_O = V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16540 | | SN74AHC16540 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 4.8 | 7 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 4.8 | 7 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PZH}$* | OE | Y | $C_L$ = 15 pF | | 6.8 | 10.5 | 1 | 12.5 | 1 | 12.5 | ns |
| $t_{PZL}$* | | | | | 6.8 | 10.5 | 1 | 12.5 | 1 | 12.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6.8 | 10.5 | 1 | 12.5 | 1 | 12.5 | ns |
| $t_{PLZ}$* | | | | | 6.8 | 10.5 | 1 | 12.5 | 1 | 12.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.3 | 10.5 | 1 | 12 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.3 | 10.5 | 1 | 12 | 1 | 12 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8 | 14 | 1 | 16 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 8 | 14 | 1 | 16 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8 | 15.4 | 1 | 17.5 | 1 | 17.5 | ns |
| $t_{PLZ}$ | | | | | 8 | 15.4 | 1 | 17.5 | 1 | 17.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16540 | | SN74AHC16540 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.7 | 5 | 1 | 6 | 1 | 6 | ns |
| $t_{PHL}$* | | | | | 3.7 | 5 | 1 | 6 | 1 | 6 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.7 | 7.2 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PZL}$* | | | | | 4.7 | 7.2 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.5 | 6.8 | 1 | 8 | 1 | 8 | ns |
| $t_{PLZ}$* | | | | | 4.5 | 6.8 | 1 | 8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.2 | 7 | 1 | 8 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5.2 | 7 | 1 | 8 | 1 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 6.2 | 9.2 | 1 | 10.5 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6 | 8.8 | 1 | 10 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6 | 8.8 | 1 | 10 | 1 | 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74AHC16540 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | | MIN | MAX | | | |
| $t_{sk(o)}$ | A | Y | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHC16540 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.7 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

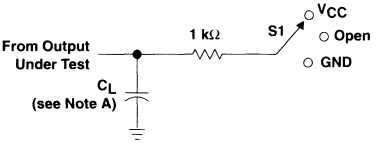
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 12 | pF |

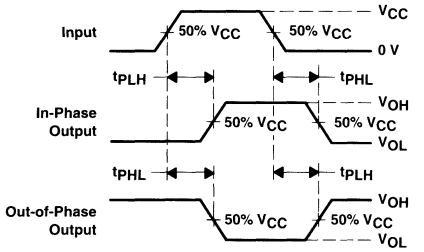
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION

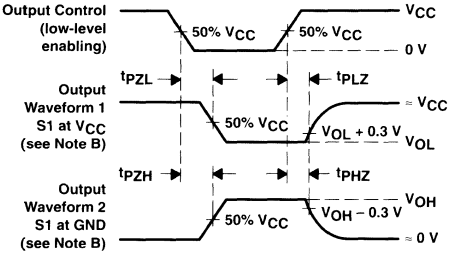



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



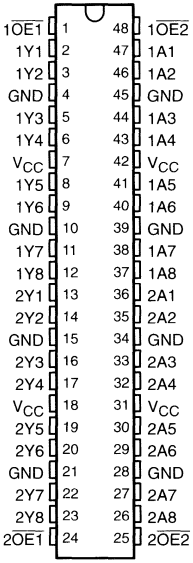

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- **Inputs Are TTL-Voltage Compatible**
- **Members of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHCT16540 . . . WD PACKAGE**
**SN74AHCT16540 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

These 16-bit buffers and bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

The SN54AHCT16540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16540 is characterized for operation from –40°C to 85°C.

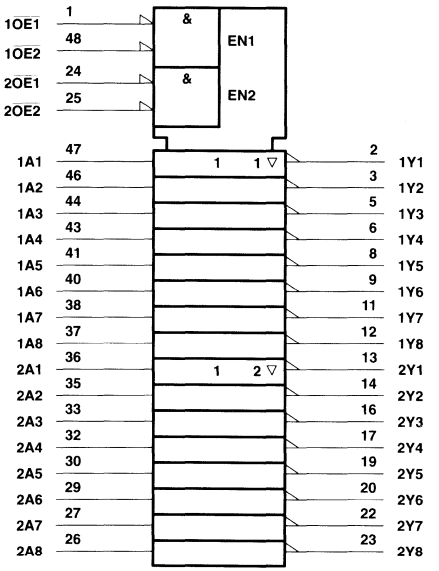
**FUNCTION TABLE**
**(each 8-bit section)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

PRODUCT PREVIEW

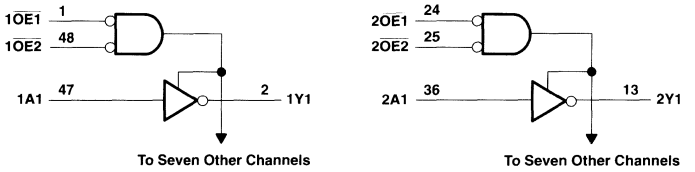
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 89°C/W
DL package . . . . . 94°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† *Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | SN54AHCT16540 | | SN74AHCT16540 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT16540 | | SN74AHCT16540 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | µA |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | µA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHCT16540 | | SN74AHCT16540 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 4 | 6 | 1 | 7.5 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 4 | 6 | 1 | 7.5 | 1 | 7.5 | |
| $t_{PZH}$* | OE | Y | $C_L$ = 15 pF | | 5.5 | 8 | 1 | 9 | 1 | 9 | ns |
| $t_{PZL}$* | | | | | 5.5 | 8 | 1 | 9 | 1 | 9 | |
| $t_{PHZ}$* | OE | Y | $C_L$ = 15 pF | | 5 | 8 | 1 | 9 | 1 | 9 | ns |
| $t_{PLZ}$* | | | | | 5 | 8 | 1 | 9 | 1 | 9 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 6 | 8.5 | 1 | 10 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 6 | 8.5 | 1 | 10 | 1 | 10 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 7.5 | 11 | 1 | 12 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.5 | 11 | 1 | 12 | 1 | 12 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 8 | 11 | 1 | 12 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 8 | 11 | 1 | 12 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74AHCT16540 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | | MIN | MAX | | | |
| $t_{sk(o)}$ | A | Y | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

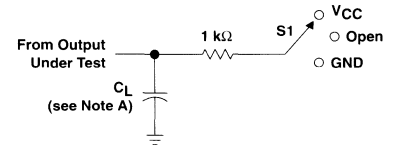
| PARAMETER | | SN74AHCT16540 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.5 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

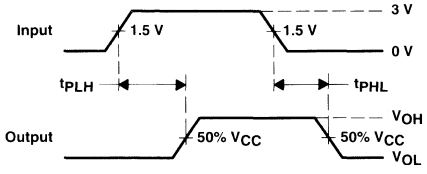
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 12 | pF |

## PARAMETER MEASUREMENT INFORMATION

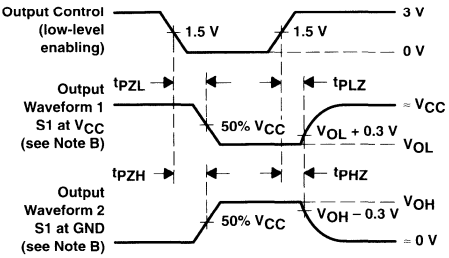



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

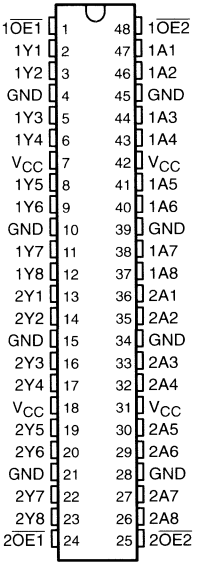
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V $V_{CC}$**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHC16541 . . . WD PACKAGE**
**SN74AHC16541 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'AHC16541 are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

The SN54AHC16541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16541 is characterized for operation from –40°C to 85°C.

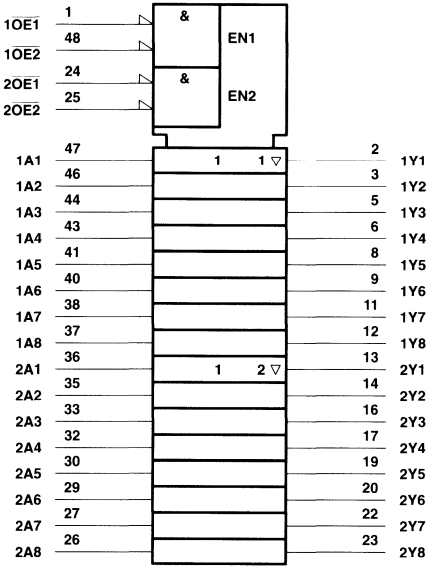
**FUNCTION TABLE**
**(each 8-bit section)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

PRODUCT PREVIEW

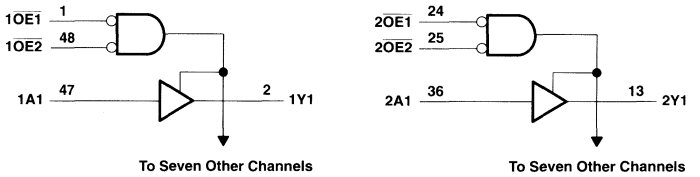
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 89°C/W
DL package . . . . . 94°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | | SN54AHC16541 | | SN74AHC16541 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC16541 | | SN74AHC16541 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | Data inputs | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| | Control inputs | | | | | ±0.1 | | ±1 | | ±1 | |
| $I_{OZ}$ | | $V_O = V_{CC}$ or GND, $V_I$ ($\overline{OE}$) = $V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| $C_o$ | | $V_O = V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16541 | | SN74AHC16541 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 5 | 7 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PHL}$* | | | | | 5 | 7 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 6 | 10.5 | 1 | 11 | 1 | 11 | ns |
| $t_{PZL}$* | | | | | 6 | 10.5 | 1 | 11 | 1 | 11 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7 | 11 | 1 | 12 | 1 | 12 | ns |
| $t_{PLZ}$* | | | | | 7 | 11 | 1 | 12 | 1 | 12 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 7.5 | 10.5 | 1 | 12 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.5 | 10.5 | 1 | 12 | 1 | 12 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8 | 14 | 1 | 16 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 8 | 14 | 1 | 16 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 9 | 15.4 | 1 | 17.5 | 1 | 17.5 | ns |
| $t_{PLZ}$ | | | | | 9 | 15.4 | 1 | 17.5 | 1 | 17.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC16541 | | SN74AHC16541 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 3.5 | 5 | 1 | 6 | 1 | 6 | ns |
| $t_{PHL}$* | | | | | 3.5 | 5 | 1 | 6 | 1 | 6 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.7 | 7.2 | 1 | 8.5 | 1 | 8.5 | ns |
| $t_{PZL}$* | | | | | 4.7 | 7.2 | 1 | 8.5 | 1 | 8.5 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 7.5 | 1 | 8 | 1 | 8 | ns |
| $t_{PLZ}$* | | | | | 5 | 7.5 | 1 | 8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5 | 7 | 1 | 8 | 1 | 8 | ns |
| $t_{PHL}$ | | | | | 5 | 7 | 1 | 8 | 1 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 6.2 | 9.2 | 1 | 10.5 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6 | 8.8 | 1 | 10 | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 6 | 8.8 | 1 | 10 | 1 | 10 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74AHC16541 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | | MIN | MAX | | | |
| $t_{sk(o)}$ | A | Y | 3.3 V ± 0.3 V | | 1.5 | | 1.5 | ns |
| | | | 5 V ± 0.5 V | | 1 | | 1 | |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHC16541 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.7 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

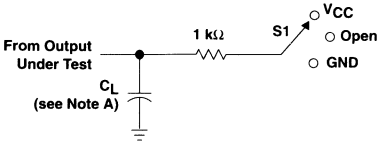
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 12 | pF |

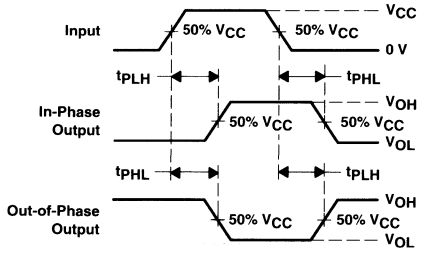
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION

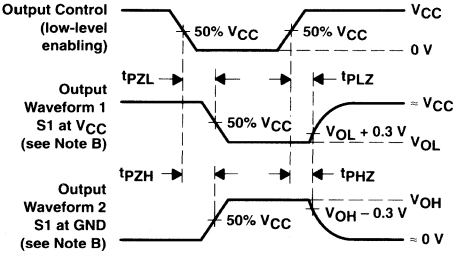



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES



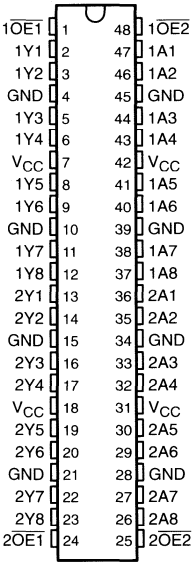

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHCT16541 . . . WD PACKAGE**
**SN74AHCT16541 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'AHCT16541 are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

The SN54AHCT16541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16541 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each 8-bit section)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

PRODUCT PREVIEW

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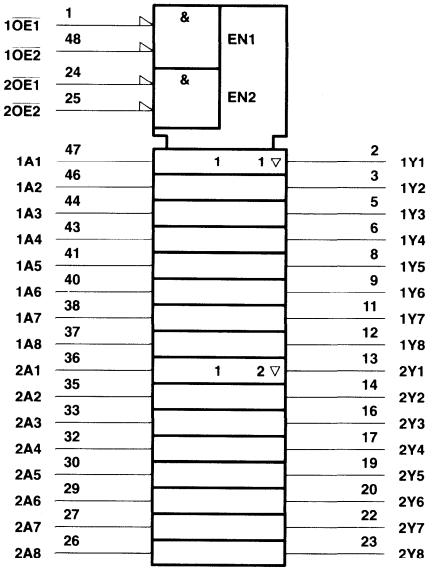
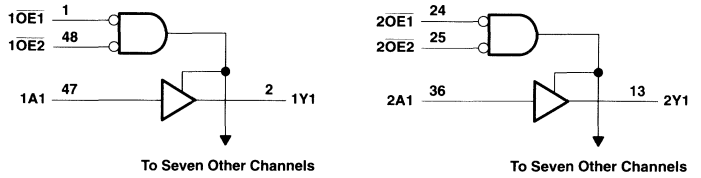
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 89°C/W
DL package . . . . . 94°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | SN54AHCT16541 | | SN74AHCT16541 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT16541 | | SN74AHCT16541 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | µA |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | µA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

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### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHCT16541 | | SN74AHCT16541 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$* | A | Y | $C_L$ = 15 pF | | 4.1 | 6 | 1 | 6.5 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 3.7 | 5.5 | 1 | 6.5 | 1 | 6.5 | |
| $t_{PZH}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5 | 7 | 1 | 8 | 1 | 8 | ns |
| $t_{PZL}$* | | | | | 5 | 7 | 1 | 8 | 1 | 8 | |
| $t_{PHZ}$* | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.5 | 7 | 1 | 8 | 1 | 8 | ns |
| $t_{PLZ}$* | | | | | 4.5 | 7 | 1 | 8 | 1 | 8 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 6.2 | 8.5 | 1 | 9.5 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 6 | 8.5 | 1 | 9.5 | 1 | 9.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 7.5 | 10 | 1 | 12 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.5 | 10 | 1 | 12 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7 | 10 | 1 | 12 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 7 | 10 | 1 | 12 | 1 | 12 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74AHCT16541 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | MIN | MAX | |
| | | | | MIN | MAX | | | |
| $t_{sk(o)}$ | A | Y | 5 V ± 0.5 V | | 1 | | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHCT16541 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.6 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

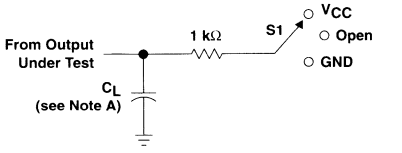
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 12 | pF |

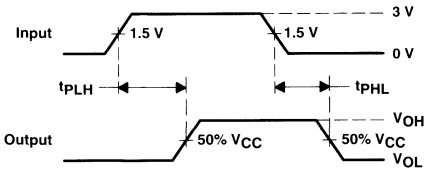
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION

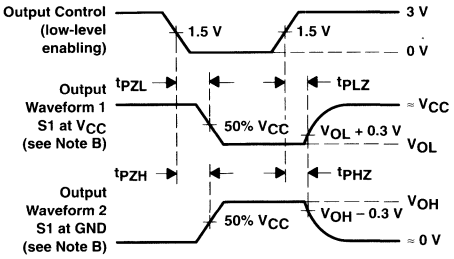



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

## Contents

# *Advanced High-Speed CMOS (AHC) Logic Family*

SCAA034A
June 1997

TEXAS INSTRUMENTS

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## Introduction

The Texas Instruments (TI™) advanced high-speed CMOS (AHC) logic family provides a natural migration for high-speed CMOS (HCMOS) users who need more speed for low-power, and low-drive applications. Unlike many other advanced logic families, AHC does not have the drawbacks that come with higher speed, e.g., higher signal noise and power consumption. The AHC logic family consists of gates, medium-scale integrated circuits, and octal functions fabricated using the EPIC™ process that features higher performance than the HCMOS HC product family at comparable cost.

This application report introduces the AHC logic family characterization information to supplement the AHC/AHCT Logic Advanced High-Speed CMOS Data Book, literature number SCLD003A. The additional information is to aid design engineers in more accurately designing their digital logic systems. The focus is on the family's features and benefits, product characteristics, and design guidelines. This application report is divided into sections, each dealing with a specific characteristic of the AHC logic family. This application report focuses on the AHC logic family and compares it to the HC family.

The main topics discussed are:

- High-Speed CMOS (HC)
- Advanced High-Speed CMOS (AHC)
- Protection Circuitry
- AC Performance
- Power Considerations
- Input Characteristics
- Output Characteristics
- Signal Integrity
- AHC Versus HC
- Advanced Packaging
- Microgate Logic

For more information on TI's AHC logic products, please contact your local TI field sales office or an authorized distributor, or call TI at 1-800-336-5236.

## High-Speed CMOS (HC)

HC has the following characteristics:

- The HC family covers a wide range of applications: low power drain for low-speed systems, and a slightly higher drain for higher-speed systems.
- The HC family has ac parameters ensured at supply voltages of 2 V, 4.5 V, and 6 V over the full operating temperature range into a 50-pF load. The TTL compatible version, HCT, is specified for a 4.5-V to 5.5-V $V_{CC}$ range.
- In HC, only the gates that are switching contribute to the dynamic system power. This reduces the size of the power supply required, thus providing lower system cost and higher reliability through lower heat dissipation.
- HC devices are ideal for battery-operated systems, or systems requiring battery backup because there is virtually no static power dissipation.
- Improved noise immunity is due to the rail-to-rail ($V_{CC}$-to-ground) output voltage swings.
- HC devices are warranted for operation over an extended temperature range of –40°C to 85°C.

## Advanced High-Speed CMOS (AHC)

AHC can be used for higher-speed applications. Some advantages of using AHC over HC are:

- The AHC logic family is almost three times faster than the HC family. The AHC logic family has a typical propagation delay of about 5.2 ns.
- The AHC logic family allows designers to combine the low-noise characteristics of HCMOS devices with today's performance levels without the overshoot/undershoot problems typical of higher-drive devices.
- The AHC family has lower power consumption than the HC family.
- The output drive is ±8 mA at 5-V $V_{CC}$ and ±4 mA at 3.3-V $V_{CC}$.
- AHC devices are available in D and DW (SOIC), DB (SSOP), N (PDIP), PW (TSSOP), and DGV (TVSOP) packages. Selected AHC devices are available in military versions (SN54AHCxx).
- Microgate Logic (single-gate) versions that simplify routing are also available.

## Protection Circuitry

Electrostatic discharge (ESD) and latchup are two traditional causes of CMOS device failure. To protect AHC devices from ESD and latchup, additional circuitry has been implemented at the inputs and outputs of each device.

### Electrostatic Discharge

ESD occurs when a buildup of static charges on one surface arcs through a dielectric to another surface that has the opposite charge. The end effect is the ESD causes a short between the two surfaces. These damaged devices might pass normal data sheet tests, but eventually fail. The input and output protection circuitry designed by TI provides immunity to over 2000 V in the human-body-model test, over 200 V in the machine-model test, and over 1000 V in the charged-device model test.

Figure 1 shows the circuitry implemented to provide protection for the input gates against ESD. The primary protection device is a low-voltage-triggered silicon-controlled rectifier (LVTSCR). During an ESD event, most of the current is diverted through the LVTSCR. Additional protection is provided by the resistor and secondary clamp transistors, which break down during an ESD event and protect the gate oxides.

Figure 2 shows how the LVTSCR protects an output.

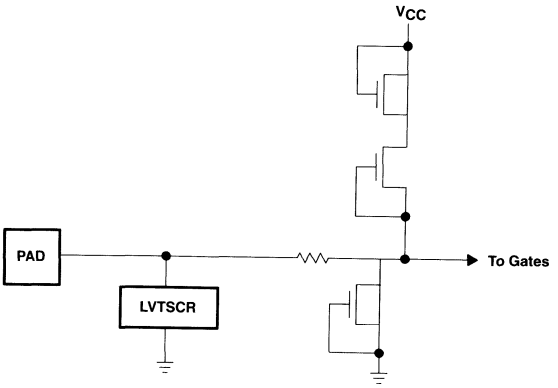



**Figure 1. ESD Input Protection Circuitry**

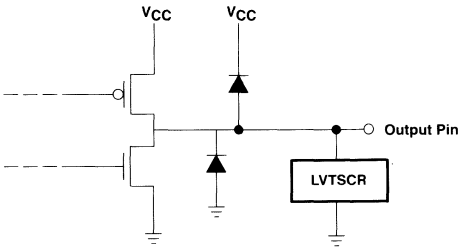



**Figure 2. ESD Output Protection Circuitry**

### Latchup Protection

Internal to almost all CMOS devices are two parasitic bipolar transistors; one p-n-p and one n-p-n. Figure 3 shows the cross section of a typical CMOS inverter with the parasitic bipolar transistors. As shown in Figure 4, these parasitic bipolar transistors are naturally configured as a thyristor or a silicon-controlled rectifier (SCR). These transistors conduct when one or more of the p-n junctions become forward biased. When this happens, each parasitic transistor supplies the necessary base current for the other to remain in saturation. This is known as the latchup condition and could destroy the device if the supply current is not limited.

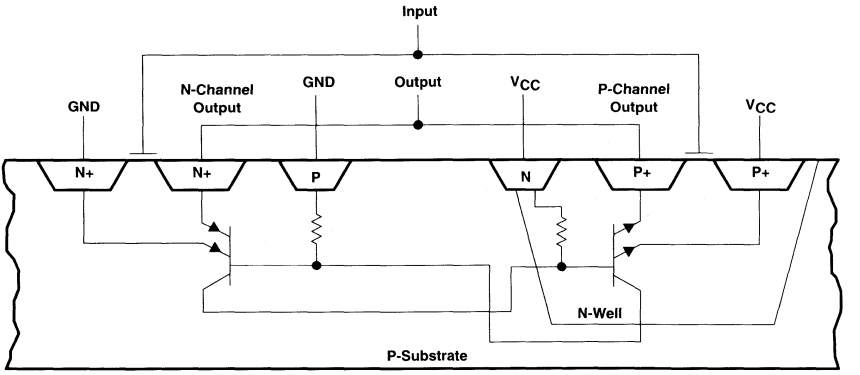



**Figure 3. Parasitic Bipolar Transistors in CMOS**

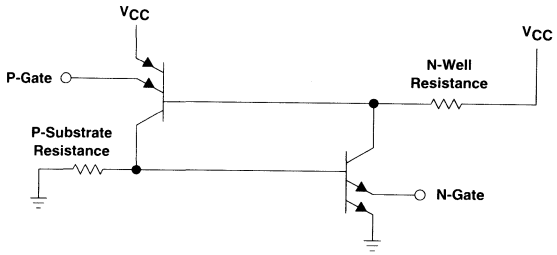



**Figure 4. Schematic of Parasitic SCR Showing P-Gate and N-Gate Electrodes Connected**

A conventional thyristor is fired (turned on) by applying a voltage to the base of the n-p-n transistor, but the parasitic CMOS thyristor is fired by applying a voltage to the emitter of either transistor. One emitter of the p-n-p transistor is connected to an emitter of the n-p-n transistor, which is also the output of the CMOS gate. The other two emitters of the p-n-p and the n-p-n transistors are connected to $V_{CC}$ and ground, respectively. Therefore, to trigger the thyristor there must be a voltage greater than $V_{CC}$ + 0.5 V or less than –0.5 V and there has to be sufficient current to cause the latchup condition.

Latchup cannot be completely eliminated. The alternative is to prevent the thyristor from triggering. TI has improved the circuit design by adding an additional diffusion or guard ring. The guard ring provides isolation between the device pins and any p-n junction that is not isolated by any transistor gate.

## Switching Characteristics

The switching characteristics of the AHC are similar to those of the AHCT in terms of the operating conditions and limits, except for the AHCT input TTL compatibility. Table 1 gives the performance figures for the HC/HCT and the AHC/AHCT logic parts. Individual data sheets provide parameter values for the AHC and the AHCT devices for different values of operating free-air temperature, number of outputs switching, and load capacitance.

**Table 1. HC and AHC Performance Comparison (Typical Values)**

| DEVICE | SN74HC | SN74HCT | SN74AHC | SN74AHCT |
|---|---|---|---|---|
| 244 buffer | 13 ns | 15 ns | 5.8 ns | 5.4 ns |
| 245 transceiver | 15 ns | 14 ns | 5.8 ns | 4.5 ns |
| 373 latch | 15 ns | 20 ns | 5 ns | 5 ns |
| 374 flip-flop | 17 ns | 25 ns | 5.4 ns | 5 ns |

AHC is almost three times faster than HC.

## Power Considerations

The power dissipation of CMOS devices can be divided into three components:

- Quiescent power dissipation, $P_q$
- Transient power dissipation, $P_t$
- Capacitive power dissipation, $P_c$

The quiescent power is the product of $V_{CC}$ and the quiescent current, $I_{CC}$. The quiescent current is the reverse current through the diodes that are reverse biased. This reverse current is generally very small (a few nA), which makes the quiescent power insignificant. However, for circuits that are in static condition for long periods, the quiescent power must be considered.

The transient power is due to the current that flows only when the transistors are switching from one logic level to the other. During this time, both of the transistors are partially on, which produces a low-impedance path between $V_{CC}$ and ground that results in a current spike. The rise (or fall) time of the input signal has a direct effect on the duration of the current spike. This is because the faster the input signal passes through the transition region, the less time both transistors are partially on. The transient power is dependent on the characteristics of the transistors, the switching frequency, and the rise and fall times of the input signal. The component can be calculated using the following equation:

$$P_t = C_{pd} \times V_{CC}^2 \times f_i \quad (1)$$

Where:

$V_{CC}$ = Supply voltage (V)
$f_i$ = Input frequency (Hz)
$C_{pd}$ = Power dissipation capacitance (F)

Additional capacitive power dissipation is caused by the charging and discharging of external load capacitance and is dependent on the switching frequency. To calculate the power, the following equation can be used:

$$P_c = C_L \times V_{CC}^2 \times f_o \quad (2)$$

Where:

$V_{CC}$ = Supply voltage (V)
$f_o$ = Output frequency (Hz)
$C_L$ = External load capacitance (F)

## Power Dissipation

AHCT devices are used primarily to interface TTL output signals to CMOS inputs. To make the inputs of the AHCT devices TTL-voltage compatible, the input transistor geometries were changed. This increased the power consumption, as compared to the equivalent AHC device, if the input is kept at a level other than GND or $V_{CC}$. The increase in power consumption occurs because TTL input levels cause both transistors in the transistor pair to be partially turned on. Included in the tables for the AHCT devices is the parameter $\Delta I_{CC}$, which enables the designer to compute how much additional current the AHCT device draws per input when at a TTL-voltage level.

Figure 5 shows the relation between the supply current and the frequency of operation for the AHC245 and the AHCT245. The increase in power consumption for the AHCT is relatively insignificant.

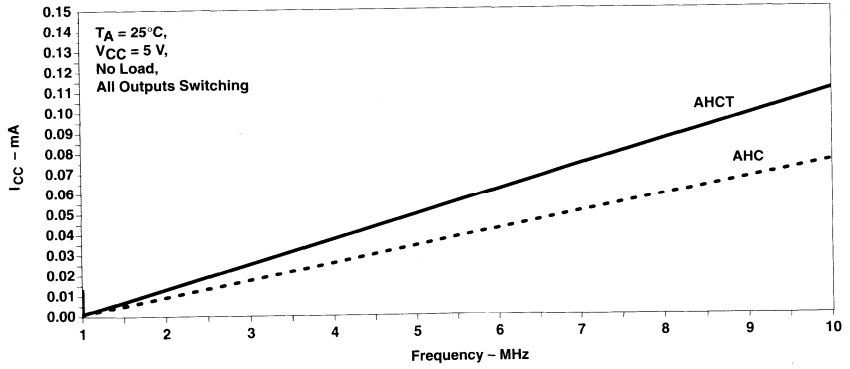



**Figure 5. $I_{CC}$ Versus Frequency**

## Input Characteristics

The AHC logic family input structure is such that the 5-V CMOS dc $V_{IL}$ and $V_{IH}$ fixed levels of 1.5 V and 3.5 V are ensured, meaning that, while the threshold voltage of 2.5 V is typically where the transition from a recognized low input to a recognized high input occurs, it is at 1.5 V and 3.5 V that the corresponding output levels are specified. For AHCT, $V_{IL}$ and $V_{IH}$ fixed levels of 0.8 V and 2 V are ensured, and the threshold voltage is 1.5 V. Figure 6 shows the characteristics for the AHC245 and the AHCT245.

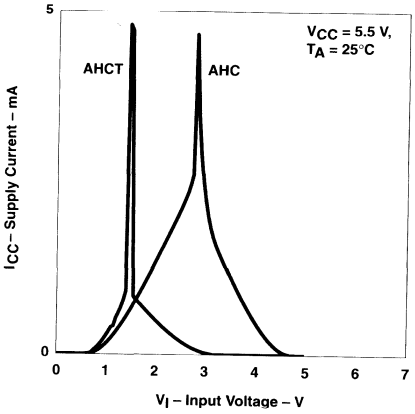



**Figure 6. Supply Current Versus Input Voltage**

## AHC Input Circuitry

The simplified AHC input circuit shown in Figure 7 consists of two transistors, sized to achieve a threshold voltage of 2.5 V. Since $V_{CC}$ is 5 V and the threshold voltage is commonly set to be centered around one-half of $V_{CC}$ in a pure CMOS input, additional circuitry to reduce the voltage level is not required and the resulting simplified input structure consists of two transistors. When the input voltage $V_I$ is low, the PMOS transistor ($Q_p$) turns on and the NMOS transistor ($Q_n$) turns off, causing current to flow through $Q_p$, resulting in the output voltage (of the input stage) to be pulled high. Conversely, when $V_I$ is high, $Q_n$ turns on and $Q_p$ turns off, causing current to flow through $Q_n$, resulting in the output voltage (on the input stage) to be pulled low.

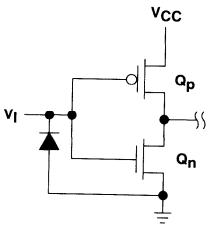
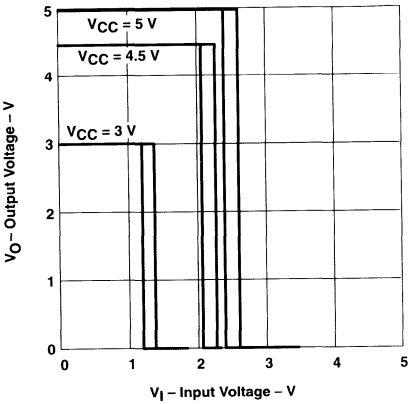



**Figure 7. Simplified Input Stage of an AHC Circuit**

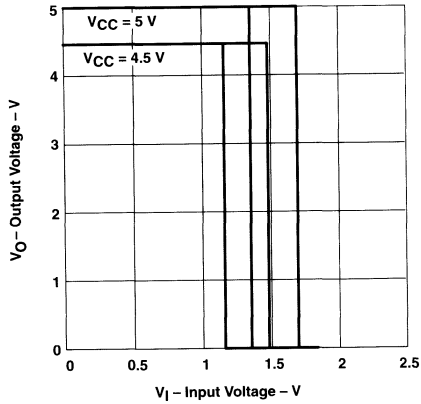
Figures 8 and 9 show the graphs of $V_O$ versus $V_I$ for the AHC04 and the AHCT04. The recommended operating range for the AHC family is from 2 V to 5.5 V. For the AHCT the recommended range is from 4.5 V to 5.5 V. Input hysteresis of typically 150 mV is included in AHC devices (300 mV in AHCT devices), which ensures the devices are free from oscillations by increasing the noise margin around the threshold voltage during low-input transitions.




$T_A$ = 25°C

| $V_{CC}$ | $V_{IHL}$ | $V_{ILH}$ |
|---|---|---|
| 5.0 V | 2.38 V | 2.49 V |
| 4.5 V | 2.13 V | 2.22 V |
| 3.0 V | 1.35 V | 1.42 V |

**Figure 8. Output Voltage Versus Input Voltage (AHC04)**




$T_A$ = 25°C

| $V_{CC}$ | $V_{IHL}$ | $V_{ILH}$ |
|---|---|---|
| 5.0 V | 1.37 V | 1.55 V |
| 4.5 V | 1.28 V | 1.46 V |

**Figure 9. Output Voltage Versus Input Voltage (AHCT04)**

### Input Current Loading

Minimal loading of the system bus occurs when using the AHC family due to the EPIC process CMOS input structure; the only loading that occurs is caused by leakage current and capacitance. Input current is low, typically less than 1 μA (see Table 2). Capacitance for transceivers can be as low as 2.5 pF for $C_i$ and 4 pF for $C_{io}$. Since both of the variables that can affect bus loading are relatively insignificant, the overall impact on bus loading on the input side using AHC devices is minimal and, depending on the logic family being used, bus loading can decrease as a result of using AHC parts.

**Table 2. Input-Current Specification**

| PARAMETER | TEST CONDITIONS | | SN74AHC245 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $I_I$ | $V_I = V_{CC}$ or GND | | | ±1 | μA |
| $I_{OZ}$† | $V_O = V_{CC}$ or GND, | $V_I = (\overline{OE}) = V_{IL}$ or $V_{IH}$ | | ±2.5 | μA |

† For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

### Supply Current Change ($\Delta I_{CC}$)

Because the input circuitry for AHC is CMOS, an additional specification, $\Delta I_{CC}$, is provided to indicate the amount of input current present when both p- and n-channel transistors are conducting (see *Power Dissipation* in the application report). Although this situation exists when a low-to-high or high-to-low transition occurs, the transition usually occurs so quickly that the current flowing while both transistors are conducting is negligible. It is more of a concern, however, when a device with a TTL output drives the AHC part. Here, a dc voltage that is not at the rail is applied to the input of the AHC device. This results in both the n-channel transistor and the p-channel transistor conducting, and a path from $V_{CC}$ to GND is established. This current is specified as $\Delta I_{CC}$ in the data sheet for each device and is measured one input at a time, with the input voltage set at $V_{CC} - 0.6$ V, while all other inputs are at $V_{CC}$ or GND. Table 3 provides the $\Delta I_{CC}$ specification, which is contained in the data sheet for the SN74AHCT245.

**Table 3. $\Delta I_{CC}$-Current Specification**

| PARAMETER | TEST CONDITIONS | SN74AHCT245 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $\Delta I_{CC}$ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND, $V_{CC}$ = 5.5 V | | 1.5 | mA |

Figure 10 is a graph of $I_I$ versus $V_I$ for the AHC245. An operating range from 0 V to 5.5 V is recommended.

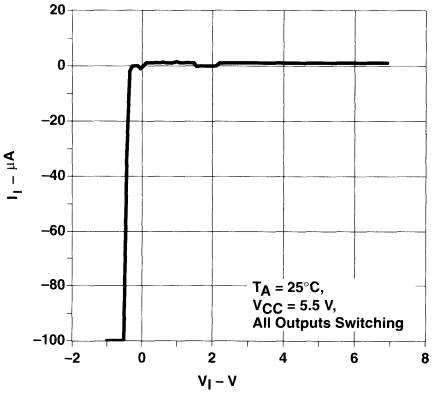



**Figure 10. Input Current Versus Input Voltage (AHC245)**

## DC Characteristics

The AHC family uses a pure CMOS output structure. The AHC family has the dc characteristics shown in Table 4. The values are measured at $T_A = 25°C$.

**Table 4. AHC DC Specifications**

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | SN74AHC245 $T_A = 25°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH} = -50\ \mu A$ | | 2 V | 1.9 | 2 | | V |
| | | | 3 V | 2.9 | 3 | | |
| | | | 4.5 V | 4.4 | 4.5 | | |
| | $I_{OH} = -4$ mA | | 3 V | 2.58 | | | |
| | $I_{OH} = -8$ mA | | 4.5 V | 3.94 | | | |
| $V_{OL}$ | $I_{OL} = 50\ \mu A$ | | 2 V | | | 0.1 | V |
| | | | 3 V | | | 0.1 | |
| | | | 4.5 V | | | 0.1 | |
| | $I_{OL} = 4$ mA, | | 3 V | | | 0.36 | |
| | $I_{OL} = 8$ mA, | | 4.5 V | | | 0.36 | |
| $I_I$ | $V_I = V_{CC}$ or GND | | 5.5 V | | | ±0.1 | μA |
| $I_{OZ}$† | $V_O = V_{CC}$ or GND, | $V_I$ ($\overline{OE}$) = $V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, | $I_O = 0$ | 5.5 V | | | 4 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | | 5 V | | 2.5 | | pF |
| $C_{io}$ | $V_I = V_{CC}$ or GND | | 5 V | | 4 | | pF |

† For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

## AHC/AHCT Output Circuitry

Figure 11 shows a simplified output stage of an AHC/AHCT circuit. When the NMOS transistor ($Q_n$) turns off and the PMOS transistor ($Q_p$) turns on and begins to conduct, the output voltage ($V_O$) is pulled high. Conversely, when $Q_p$ turns off, $Q_n$ begins to conduct and $V_O$ is pulled low. The AHC/AHCT devices have a rail-to-rail output swing to make them compatible with the HC/HCT families.

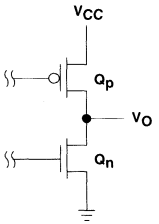



**Figure 11. Simplified Output Stage of an AHC Circuit**

### Output Drive

Figure 12 shows values for $V_{OL}$ vs $I_{OL}$, and $I_{OH}$ vs $V_{OH}$ for the AHC/AHCT245.

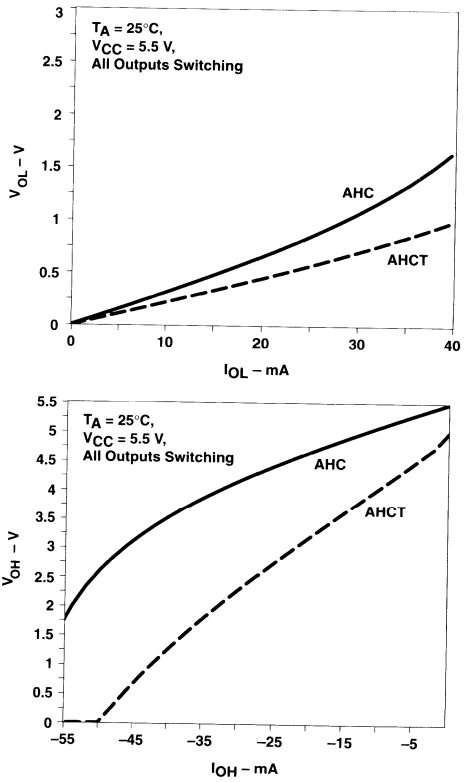



**Figure 12. AHC Output Characteristics**

### Partial Power Down

All AHC devices are 5-V input tolerant when operated at 3.3 V. To partially power down a device, no paths from the input or output pins to $V_{CC}$ exist. With the AHC family, there are no paths from the input pins to $V_{CC}$. The AHC/AHCT devices have rail-to-rail output swings to make them compatible with the HC/HCT family. The AHC/AHCT devices do not have a path from the output pins to $V_{CC}$ and can be partially powered down.

## Proper Termination of Outputs

Depending on the trace length, special consideration might need to be given to the termination of the outputs. As a general rule, if the trace length is less than four inches, no additional components are necessary to achieve proper termination. If the trace length is greater than four inches, reflections begin to appear on the line and the system might appear noisy and generate unreliable data. The solution to this is to terminate the outputs in an appropriate manner to minimize the reflections.

## Common Termination Techniques

Most transmission-line termination techniques rely on impedance matching at either the source or receiver to reduce reflections and line noise (see Figure 13). Series, thevenin, and ac techniques commonly are used and are effective methods of line termination for high-speed logic. Shunt termination is educational, but has implementation problems. Diodes can be used as a solution, but, generally, this is not a good termination technique by itself.

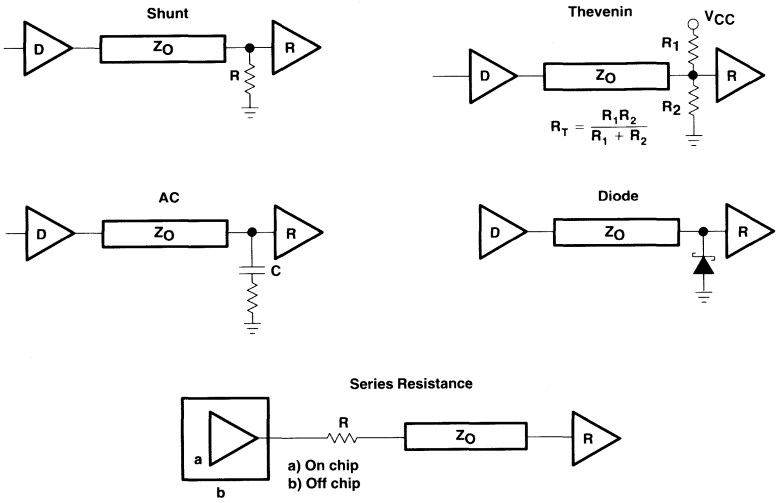



**Figure 13. Termination Techniques**

### Shunt

Shunt termination (see Figure 13) is one of the simplest termination techniques to implement. The value of the termination resistor should match the line impedance for best performance. As the transmitted signal reaches the receiver, the shunt termination drains off the current with an impedance matching the transmission line. There is no reflection, thus, no noise is retransmitted down the transmission line.

There are several disadvantages to shunt termination. Usually the line impedance is fairly low (50 Ω to 70 Ω), which requires a resistor of similar value. This causes a heavy dc current drain on the source when in the logic high state and requires a strong line driver to source the current. With the low-impedance resistor pulling to GND, the $V_{OH}$ of the transmission line is lower, reducing the noise immunity at the receiver. Additionally, having a strong pull down on the transmission line might unbalance the rising and falling edges of the signal, causing the falling edge to be faster than the rising edge, resulting in duty-cycle distortion of the signal.

### AC

AC termination utilizes the same line-impedance-matching resistor as shunt termination, except it is ac coupled with a capacitor, making a simple high-pass filter. The capacitor appears to be a short circuit during signal transitions when termination is needed, but eliminates the dc component of the current drain.

AC termination (see Figure 13) has the precise termination advantages of shunt termination, but reduces the disadvantages of dc current drain and waveform distortion. At each transition of the signal, the capacitor charges up to the voltage level necessary to maintain zero volts across the resistor. During the arrival of the next input transition, the signal drives the full value of the resistor until the capacitor can again recharge.

It is recommended that the resistor value be equivalent to the line impedance. The ideal capacitor value varies with line impedance, edge rate, and desired signal quality. The values are not critical, but tests have shown that with TI logic, a value of 50 pF for the capacitor is a good compromise. Increasing the capacitance value to 200 pF improves signal quality, but sacrifices power dissipation. Reducing the value to 47 pF lowers the power dissipation, but sacrifices signal quality. Values below 47 pF give a very high frequency response to the filter and tend to be ineffective for line termination. Values above 200 pF add power dissipation without additional signal quality improvement. AC termination is excellent for use with clock drivers, cables, backplanes, distributed loads, and many other applications. The combined cost of the capacitor, resistor, and real estate for each line frequently precludes general use for on-board bus termination.

### Thevenin

Thevenin termination (see Figure 13) attempts to correct the dc problems of shunt termination by reducing the dc load of the termination and pulling the signal closer to the center of the transition. For high-speed logic, it is best to center the dc level at a logic high (>2.0 V) to avoid holding the input at the input threshold (toggle point » 1.5 V). Under this condition, if the driver shuts off (high Z), the input pulls up rather than causing oscillations from logic uncertainties.

A disadvantage of thevenin termination is the dc leakage from $V_{CC}$ to GND through the terminator. Using thevenin termination to match a 50- or 70-Ω line requires a parallel resistance that is low enough to pass considerable current. Thevenin is commonly used on backplanes, cables, and other long transmission lines. Some applications, such as backplanes, might require termination at both ends of the transmission line.

### Diode

Diode termination (see Figure 13) simply clips the undershoot of a high-to-low transitioning signal and thereby reduces the line reflection. Diode termination can be effective if the cause of the problem is undershoot and the frequency response of the diode is considerably higher than the transition frequency of the signal.

With very-high-speed logic families, such as TI's, the frequency response of the output-signal transition can reach 400 MHz and beyond. At these frequencies, the effectiveness of diode termination is limited due to the frequency response of the terminator. While some benefit might be realized with diode termination, the inductances, capacitances, and frequency response of the diode and diode connections probably make the termination scheme less effective when used at high frequencies.

The internal parasitic clamp diode to ground, found on the inputs and outputs of all CMOS logic, bleed off some of the overshoot current, but this parasitic clamp does not have the necessary frequency response to perform effective diode termination in high-speed applications. Diode termination frequently is used on backplanes and long cables, possibly in conjunction with another form of line termination.

### Series (Source Terminated)

Series termination reduces the output edge rate of the driver, the switching amplitude of the signal, and the charge injected into the transmission line. This has significant benefits by reducing signal line noise and electromagnetic interference (EMI). Series termination adds a series resistor at the output of the line driver, effectively increasing the source impedance of the driver (see Figure 13). When using series termination with distributed loads, care must be taken that the combined output impedance of the driver and series resistor is small enough to allow first incident-wave switching. If the output impedance becomes too high, the step that is seen in the output transition does not toggle the components at the near end of the transmission line until the signal passes down the line and returns to the source, causing an unnecessary propagation delay. Series termination is the most commonly used form of termination and is found on circuit boards, cables, and in most other applications.

Table 5 provides a comparison of the five termination techniques.

**Table 5. Termination Techniques Summary**

| TECHNIQUE | ADDITIONAL DEVICES | POWER INCREASE | DELAY | HOLDS DEFINED LEVEL | IDEAL VALUE† | COMMENTS |
|---|---|---|---|---|---|---|
| Shunt | 1 | Significant | No | Yes | $R = Z_O$ | Low dc noise margin |
| Thevenin | 2 | Yes | No | Yes | $R_1 = R_2 = 2Z_O$ | Good for backplanes due to maintaining drive current |
| AC | 2 | Yes | No | No | $R = Z_O$<br>$60 < C < 330$ pF | Increase in frequency and power |
| Series resistor on device | 0 | No | Small | No | $25 = < R = < 33\ \Omega$ | Good undershoot clamping; useful for point-to-point driving |
| Diode | 1 | No | No | No | NA | Good undershoot clamping; useful for standard backplane terminations |

† Symbols are defined in Figure 13.

## Signal Integrity

System designers often are concerned with the performance of a device when the outputs are switched. The most common method of assessing this is by observing the impact on a single output when multiple outputs are switched.

### Simultaneous Switching

In a digital circuit, when multiple outputs switch, the current through the ground or $V_{CC}$ terminals changes rapidly. As this current flows through the ground (or $V_{CC}$) return path, it develops a voltage across the parasitic inductance of the bond wire and the package pin. The phenomenon is called simultaneous switching noise. Figure 14 shows the equivalent circuit of a typical CMOS output buffer stage with the package parasitics and the external load. The parasitic components that affect the ground bounce are inductance and resistance of the ground bond wire and pin, inductance and resistance of the output bond wire and pin, and load impedance. For the first-order analysis, the parasitics associated with the $V_{CC}$ terminal can be ignored. Also, the external ground plane is assumed to be ideal.

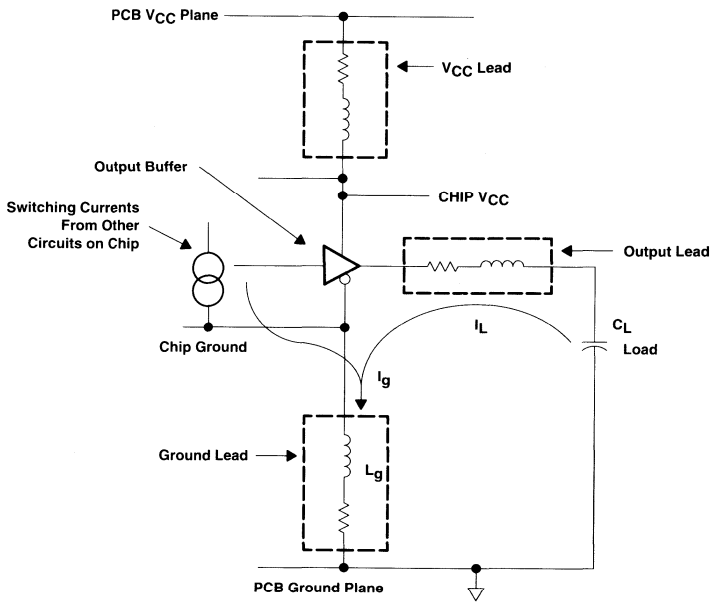



**Figure 14. Output Buffer With External Parasitics**

During the output high-to-low transition, the sum of the output load current and all switching current through the internal gates of the device flows through the ground lead. The rate of change of this current (di/dt) develops a voltage drop across the ground lead inductance and causes a positive ground bounce or an overshoot in an otherwise quiet ground. This positive ground bounce is normally followed by an undershoot coincident with the voltage waveform on the output terminal. The amplitudes of both the positive and the negative ground bounce are a function of $L_g * di/dt$ and of the number of outputs switching simultaneously (SS noise). The ground-bounce phenomenon can be clearly observed at an unswitched low output of a device by switching several other outputs simultaneously from logic high to low. Figure 15 shows the typical output voltage transition and the corresponding ground bounce, as observed at the unswitched low output. Positive ground bounce is primarily the result of the rate of change of current (di/dt) through the ground lead inductance. The rate is determined by the rate at which the gate-to-source voltage ($V_{gs}$) of the sink transistor changes. During the early part of the fall time, the ground voltage rises while the output voltage falls, forcing the sink transistor into the linear region. The transistor then behaves like a resistor $R_{on}$ (the on-state resistance of the transistor in the linear region). For the remainder of the output voltage excursion, the equivalent circuit at the output can be treated like a resonant L-C-R circuit formed by the ground and the output lead inductance, load capacitance, and the total resistance in the loop, which includes $R_{on}$. The oscillation frequency is determined by the net values of L and C, while damping is determined by L and the total resistance in the loop. Ground bounce also is generated during the output low-to-high transition. However, the magnitude of this ground bounce is much smaller because of the absence of load current in the ground lead.

Ground and $V_{CC}$ bounce cannot be eliminated, but they can be minimized by controlling edge rates and reducing output swing. Ground bounce depends on many factors, with device speed being one of the more important influences. As device speed goes up, the rate of change of current in the parasitic inductances increases and the related switching noise goes up. Due to this correlation between speed and ground bounce, high-speed logic families arouse increased concern over noise due to simultaneous switching of outputs.

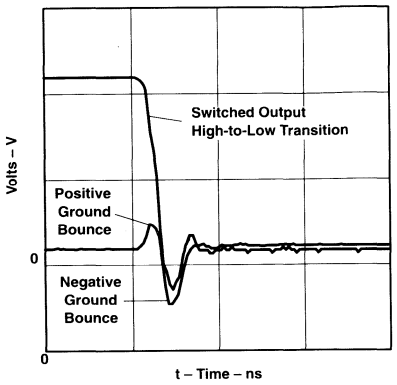



**Figure 15. Simultaneous-Switching-Noise Waveform**

### Ground-Bounce Measurement

There is no industry standard for measuring ground bounce. However, the method most commonly used by IC vendors and customers is based on observing the disturbance of a logic-low level on an unswitched output of a multiple-output device while switching all other outputs from a high to a low state. Figure 16 shows the schematic for measuring ground bounce on a device such as the AHC244 octal buffer. One output is in the low state while the outputs are switched simultaneously. The load on each output consists of a 50-pF capacitor. Two outputs are connected to the oscilloscope: one for observing the high-to-low transition of a switched output and the other for observing the ground bounce on the quiet output.

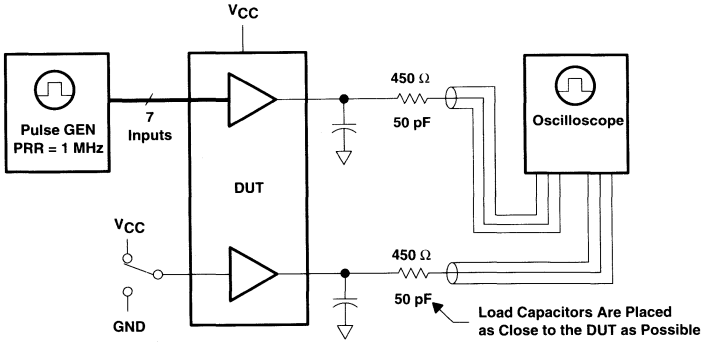



**Figure 16. Ground-Bounce Test Circuit**

With careful layout, proper bypassing to filter out high-frequency noise, and good oscilloscope probes, it is possible to observe the ground bounce on the internal ground of the chip by observing the voltage at the unswitched low output, whose sink transistor operates in the linear region and provides a Kelvin connection to the chip ground.

One technique to reduce the impact of simultaneous switching on a device is to increase the number of power and GND pins. The strategy is to disperse them throughout the chip (see the *Advanced Packaging* section of this application report). For a complete discussion of simultaneous switching, refer to TI's *Simultaneous Switching Evaluation and Testing*, in the *Advanced CMOS Logic Designer's Handbook*, literature number SCAA001B.

## AHC Versus HC

A speed-versus-current-drive comparison between the AHC and HC families is shown in Figure 17. The speed for the AHC is much higher than the HC. Both these products support low-drive applications.

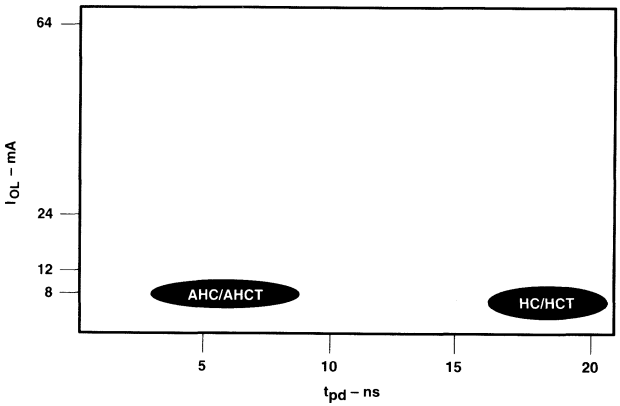



**Figure 17. AHC/AHCT and HC Family Positioning**

Table 6 shows the features of HC and AHC families. AHC provides much higher speeds with no noise penalty.

**Table 6. AHC and HC Features (Typical Values)**

| PRODUCT FAMILY | | AHC | HC |
|---|---|---|---|
| Technology | | CMOS | CMOS |
| 5-V tolerant† | | Yes (inputs) | Yes (inputs) |
| Octals and gates | | Yes | Yes |
| Widebus™ (16-bit products) | | Yes | No |
| Bus hold | | Yes | No |
| Damping resistors | | No | No |
| $I_{CC}$ | '245 | 40 μA | 80 μA |
| DC output drive | | –8 mA/8 mA | –8 mA/8 mA |
| $t_{pd}$ | '245 | 5 ns | 18 ns |
| $C_i$ | '245 | 2.5 pF | 3 pF |
| $C_{io}$ | '245 | 8 pF | 10 pF |

† When operated at 3.3 V

## Advanced Packaging

Figure 18 shows a comparison of packages in which AHC devices are available; for ease of analysis, 14-pin packages and 20-pin packages are included. Figure 19 is not an all-inclusive list of pin counts and corresponding packages, e.g., the TSSOP package is available in both 14-pin and 20-pin format. The TVSOP package, which has a lead pitch of 0.4 mm (16 mil) and a device height of 1.2 mm, is also available in the AHC family. Continued advancements in packaging are making more functionality possible with smaller space requirements.

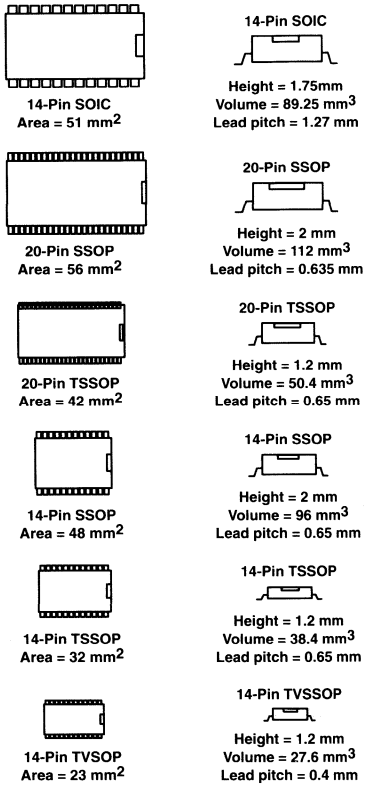



**Figure 18. AHC Packages**

Figure 19 shows a typical pinout structure for the 20-pin SSOP for the SN74AHC245. This provides for simultaneous switching improvements (see the *Signal Integrity* section of this application report).

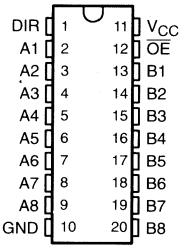



**Figure 19. SN74AHC245 Pinout**

For a comprehensive listing and explanation of TI's packaging options, consult the *Semiconductor Group Package Outlines Reference Guide*, literature number SSYU001C.

## Microgate Logic

The Microgate Logic device is a single gate that is used instead of the two-, four-, or six-gate versions. The advantages of Microgate Logic are:

- Simplified circuit routing
- Help in ASIC modification
- 3.5-ns typical propagation delay

Microgate Logic is available in CMOS (AHC) and TTL (AHCT) versions. The AHC versions are compatible with Toshiba's TC7SHxx series. Figure 20 shows the pinout of the SN74AHC1G00.

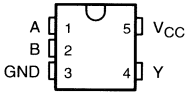



**Figure 20. 5-Pin Microgate Logic Pinout**

## Acknowledgment

The author of this report is Shankar Balasubramaniam.

# *CMOS Power Consumption and $C_{pd}$ Calculation*

SCAA035B
June 1997

TEXAS INSTRUMENTS

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## Contents



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## Introduction

Reduction of power consumption makes a device more reliable. The need for devices that consume a minimum amount of power was a major driving force behind the development of CMOS technologies. As a result, CMOS devices are best known for low power consumption. However, for minimizing the power requirements of a board or a system, simply knowing that CMOS devices may use less power than equivalent devices from other technologies does not help much. It is important to know not only how to calculate power consumption, but also to understand how factors such as input voltage level, input rise time, power-dissipation capacitance, and output loading affect the power consumption of a device. This application report addresses the different types of power consumption in a CMOS logic circuit, focusing on calculation of power-dissipation capacitance ($C_{pd}$), and, finally, the determination of total power consumption in a CMOS device.

The main topics discussed are:

- Power-consumption components
- Static power consumption
- Dynamic power consumption
- Power-dissipation capacitance ($C_{pd}$) in CMOS circuits
- $C_{pd}$ comparison among different families
- Power economy
- Conclusion

## Power-Consumption Components

High frequencies impose a strict limit on power consumption in computer systems as a whole. Therefore, power consumption of each device on the board should be minimized. Power calculations determine power-supply sizing, current requirements, cooling/heatsink requirements, and criteria for device selection. Power calculations also can determine the maximum reliable operating frequency.

Two components determine the power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

CMOS devices have very low static power consumption, which is the result of leakage current. This power consumption occurs when all inputs are held at some valid logic level and the circuit is not in charging states. But, when switching at a high frequency, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption.

This application report addresses power consumption in CMOS logic families (5 V and 3.3 V) and describes the methods for evaluating both static and dynamic power consumption. Additional information is also presented to help explain the causes of power consumption, and present possible solutions to minimize power consumption in a CMOS system.

## Static Power Consumption

Typically, all low-voltage devices have a CMOS inverter in the input and output stage. Therefore, for a clear understanding of static power consumption, refer to the CMOS inverter modes shown in Figure 1.

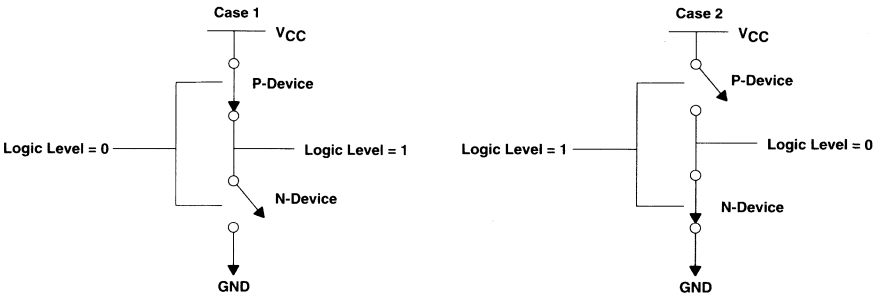



**Figure 1. CMOS Inverter Mode for Static Power Consumption**

As shown in Figure 1, if the input is at logic 0, the n-MOS device is OFF, and the p-MOS device is ON (Case 1). The output voltage is $V_{CC}$, or logic 1. Similarly, when the input is at logic 1, the associated n-MOS device is biased ON and the p-MOS device is OFF. The output voltage is GND, or logic 0. Note that one of the transistors is always OFF when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no dc current path from $V_{CC}$ to GND, the resultant quiescent (steady-state) current is zero, hence, static power consumption ($P_q$) is zero.

However, there is a small amount of static power consumption due to reverse-bias leakage between diffused regions and the substrate. This leakage inside a device can be explained with a simple model that describes the parasitic diodes of a CMOS inverter, as shown in Figure 2.

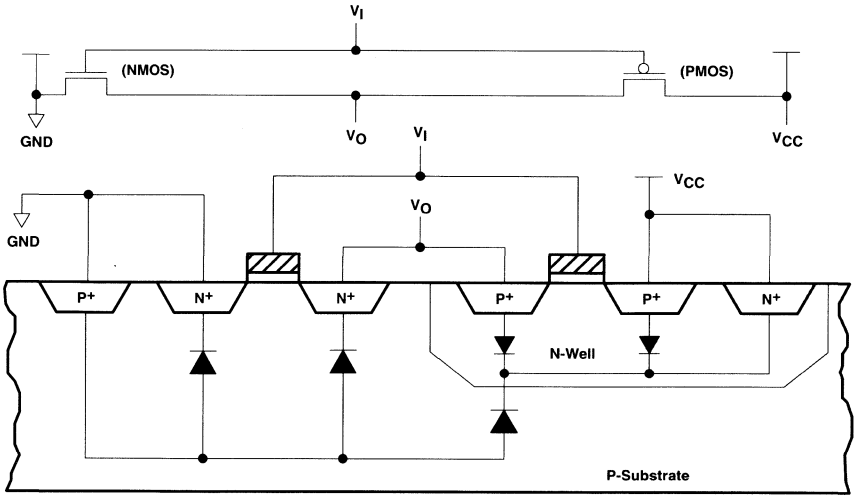



**Figure 2. Model Describing Parasitic Diodes Present in CMOS Inverter**

The source drain diffusion and N-well diffusion form parasitic diodes. In Figure 2, the parasitic diodes are shown between the N-well and substrate. Because parasitic diodes are reverse biased, only their leakage currents contribute to static power consumption. The leakage current ($I_{lkg}$)of the diode is described by the following equation:

$$I_{lkg} = i_s(e^{qV/kT} - 1) \quad (1)$$

Where:

$i_S$ = reverse saturation current
V = diode voltage
k = Boltzmann's constant ($1.38 \times 10^{-23}$ J/K)
q = electronic charge ($1.602 \times 10^{-19}$ C)
T = temperature

Static power consumption is the product of the device leakage current and the supply voltage. Total static power consumption, $P_S$, can be obtained as shown in equation 2:

$$P_S = \Sigma \text{ (leakage current)} \times \text{(supply voltage)} \quad (2)$$

Most CMOS data sheets specify an $I_{CC}$ maximum in the 10-µA to 40-µA range, encompassing total leakage current and other circuit features that may require some static current not considered in the simple inverter model.

The leakage current $I_{CC}$ (current into a device), along with the supply voltage, causes static power consumption in the CMOS devices. This static power consumption is defined as quiescent, or $P_S$, and can be calculated by equation 3.

$$P_S = V_{CC} \times I_{CC} \quad (3)$$

Where:

$V_{CC}$ = supply voltage
$I_{CC}$ = current into a device (sum of leakage currents as in equation 2)

Another source of static current is $\Delta I_{CC}$. This results when the input levels are not driven all the way to the rail, causing the input transistors to not switch off completely.

## Dynamic Power Consumption

The dynamic power consumption of a CMOS IC is calculated by adding the transient power consumption ($P_T$), and capacitive-load power consumption ($P_L$).

### Transient Power Consumption

Transient power consumption is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This is a result of the current required to charge the internal nodes (*switching current*) plus the *through current* (current that flows from $V_{CC}$ to GND when the p-channel transistor and n-channel transistor turn on briefly at the same time during the logic transition). The frequency at which the device is switching, plus the rise and fall times of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible compared to the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the IC and the charge and discharge current of the load capacitance.

Transient power consumption can be calculated using equation 4.

$$P_T = C_{pd} \times V_{CC}^2 \times f_i \times N_{SW} \quad (4)$$

Where:

$P_T$ = transient power consumption
$V_{CC}$ = supply voltage
$f_I$ = input signal frequency
$N_{SW}$ = number of bits switching
$C_{pd}$ = dynamic power-dissipation capacitance

In the case of single-bit switching, $N_{SW}$ in equation 4 is 1.

Dynamic supply current is dominant in CMOS circuits because most of the power is consumed in moving charges in the parasitic capacitor in the CMOS gates. As a result, the simplified model of a CMOS circuit consisting of several gates can be viewed as one large capacitor that is charged and discharged between the power-supply rails. Therefore, the power–dissipation capacitance ($C_{pd}$) is often specified as a measure of this equivalent capacitance and is used to approximate the dynamic power consumption. $C_{pd}$ is defined as the internal equivalent capacitance of a device calculated by measuring operating current without load capacitance. Depending on the output switching capability, $C_{pd}$ can be measured with no output switching (output disabled) or with any of the outputs switching (output enabled). $C_{pd}$ is discussed in greater detail in the next section.

## Capacitive-Load Power Consumption

Additional power is consumed in charging external load capacitance and is dependent on switching frequency. The following equation can be used to calculate this power if all outputs have the same load and are switching at the same output frequency.

$$P_L = C_L \times V_{CC}^2 \times f_O \times N_{SW} \ (C_L \text{ is the load per output}) \quad (5)$$

Where:

$P_L$ = capacitive-load power consumption
$V_{CC}$ = supply voltage
$f_O$ = output signal frequency
$C_L$ = external (load) capacitance
$N_{SW}$ = total number of outputs switching

In the case of different loads and different output frequencies at all outputs, equation 6 is used to calculate capacitive-load power consumption.

$$P_L = \Sigma(C_{Ln} \times f_{On}) \times V_{CC}^2 \quad (6)$$

Where:

$\Sigma$ = sum of n different frequencies and loads at n different outputs
$f_{On}$ = all different output frequencies at each output, numbered 1 through n (Hz)
$V_{CC}$ = supply voltage (V)
$C_{Ln}$ = all different load capacitances at each output, numbered 1 through n.

Therefore, dynamic power consumption ($P_D$) is the sum of these two power consumptions and can be expressed as shown in equation 7, equation 8 (single-bit switching), and equation 9 (multiple-bit switching with variable load and variable output frequencies).

$$P_D = P_T + P_L \tag{7}$$

$$P_D = (C_{pd} \times f_i \times V_{CC}^2) + (C_L \times f_o \times V_{CC}^2) \tag{8}$$

$$P_D = \left[(C_{pd} \times f_i \times N_{SW}) + \Sigma(C_{Ln} \times f_{On})\right] \times V_{CC}^2 \tag{9}$$

Where:

$C_{pd}$ = power-consumption capacitance (F)
$f_I$ = input frequency (Hz)
$f_{On}$ = all different output frequencies at each output, numbered 1 through n (Hz)
$N_{SW}$ = total number of outputs switching
$V_{CC}$ = supply voltage (V)
$C_{Ln}$ = all different load capacitances at each output, numbered 1 through n.

Total power consumption is the sum of static and dynamic power consumption.

$$P_{tot} = P_{(static)} + P_{(dynamic)} \tag{10}$$

## Power-Dissipation Capacitance ($C_{pd}$) in CMOS Circuits

$C_{pd}$ is an important parameter in determining dynamic power consumption in CMOS circuits. It includes both internal parasitic capacitance (e.g., gate-to-source and gate-to-drain capacitance) and *through currents* present while a device is switching and both n-channel and p-channel transistors are momentarily conducting.

### Testing Considerations

Proper setup is vital to achieving proper correlation. Some of the more important issues in performing the measurement are discussed in this section.

#### *Input Edge Rates*

When measuring $C_{pd}$, the input edge rate should be $t_r = t_f = 1$ ns from 10% to 90% of the input signal. Power-dissipation capacitance is heavily dependent on the dynamic supply current, which, in turn, is sensitive to input edge rates. As previously noted, while an input is switching, there is a brief period when both p-channel and n-channel transistors are conducting, which allows *through current* to flow from $V_{CC}$ to GND through the input stage. The amount of dynamic *through current* measured is directly proportional to the amount of time the input signal is at some level other than $V_{CC}$ or GND.

#### *Bypassing*

Any circuit must be properly bypassed to function correctly at high frequencies. The bypass capacitor between $V_{CC}$ and GND serves to reduce power-supply ripple and provides a more accurate measure of the current being drawn by the device under test. Improper bypassing can result in erratic voltage at the $V_{CC}$ pin and can disrupt the test. Texas Instruments (TI) uses a 0.1-µF bypass capacitor (from $V_{CC}$ to GND) on the test board.

#### *Pin Combination*

Different pin combinations are valid and may be chosen to best suit the application at hand. For example, it is valid to test a device with the outputs either enabled or disabled. For multisection devices, set the device so that the minimum number of sections is active. Virtually any pin combination that causes at least one output to switch at a known frequency is acceptable.

### Test Conditions

The test conditions for $C_{pd}$ calculation for any device requires the following information (an LVC device is used as an example):

| | |
|---|---|
| $V_{CC}$ | 5 V |
| Ambient temperature, $T_A$ | 25°C |
| AC bias levels | 0 V, 3.3 V |
| DC bias level | 0 V, 3.3 V |
| Input edge rates | $t_r = t_f = 1$ ns (smallest possible) |
| Input frequencies | 0.1, 1, 2, 3, ...20, 25, 30, ...75 MHz |
| $C_{pd}$ frequency | 10 MHz |
| Duty cycle | 50% |

Similarly, the test conditions for $I_{CC}$ versus frequency are also applicable to determine the $C_{pd}$ for CMOS devices. An AHC00 device is considered as an example for test conditions to calculate $C_{pd}$ through $I_{CC}$ versus frequency data and using the $C_{pd}$ equation described in the next section (*Calculating $C_{pd}$*).

| | |
|---|---|
| $V_{CC}$ | 5 V |
| Ambient temperature, $T_A$ | 25°C |
| AC bias levels | 0 V, 5V |
| DC bias level | 5 V |
| Input edge rates | $t_r = t_f = 2$ ns (smallest possible) |
| Input frequencies | 0.1, 1, 2, 3, ...20, 25, 30, ...75 MHz |
| Duty cycle | 50% |

For nontransceiver devices with 3-state outputs, testing is performed with the outputs enabled and disabled. When disabled, pullup resistors are not required. For a transceiver with 3-state outputs, testing also is performed with outputs enabled and disabled. However, in the disabled mode, 10-kΩ pullup resistors to the $V_{CC}$ power supply or to GND must be added to all inputs and outputs.

### Calculating $C_{pd}$

$C_{pd}$ is calculated by putting the device in the proper state of operation and measuring the dynamic $I_{CC}$ using a true RMS multimeter. Testing is done at an input frequency of 1 MHz to reduce the contribution of the dc supply current to the point that it can be ignored. Measurements for all devices are made at $V_{CC}$ = 5 V or 3.3 V, $T_A$ = 25°C. The test frequency must be low enough to allow the outputs to switch from rail to rail. For this reason, devices with 3-state outputs are measured at 10 MHz.

### $C_{pd}$ Measurement Procedures

For devices that have several gates in the same package (for example, AHC04 has six individual inverter circuits as shown in Figure 3), the average $C_{pd}$ per output is specified in the data sheet as a typical (TYP) value.

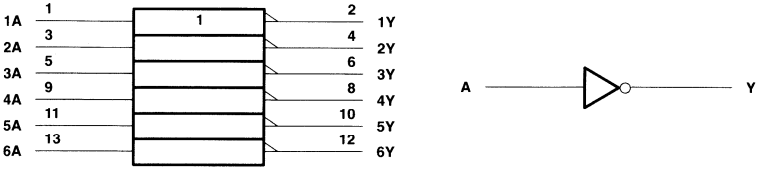



**Figure 3. Hex Inverter AHC04**

For devices that have several circuits switching simultaneously from a single clock or input (such as the AHC374 in Figure 4), switch all outputs and deduct $P_L$ for each output. In the case of multiple-output switching at different frequencies (i.e., divide counters with parallel outputs) each $P_L$ will have a different frequency factor.

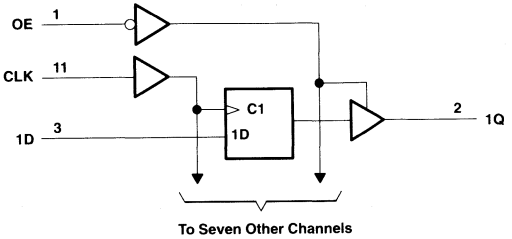



**Figure 4. Several Circuits Switching, AHC374**

In the case of devices such as ALVC, LVC, and LV, test and calculate $C_{pd}$ for both the enable and disable mode. Typically, $C_{pd}$ in the enable mode is greater than $C_{pd}$ in the disable mode ($C_{pd\_EN} > C_{pd\_DIS}$).

### Determination of $C_{pd}$ (Laboratory Testing)

In the laboratory, determine $C_{pd}$ for any device, such as AHC00, by measuring the $I_{CC}$ being supplied to the device under the conditions in the *Test Conditions* section. Figure 5 provides the $I_{CC}$ and frequency data for the AHC00 that can be used to calculate $C_{pd}$ for the device, using equation 6 with a no-load condition.

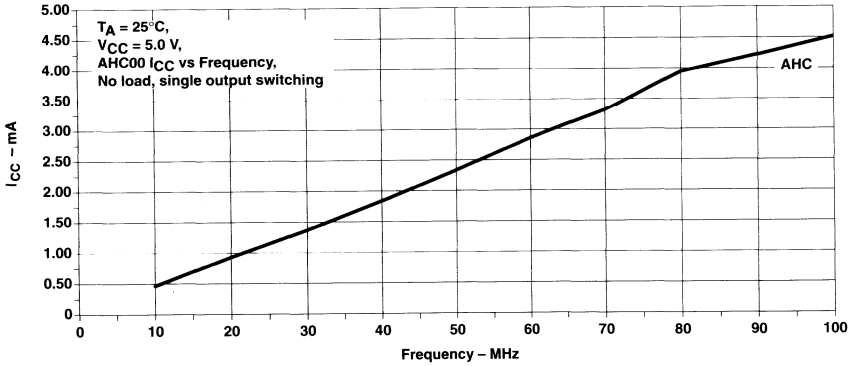



**Figure 5. $I_{CC}$ vs Frequency for AHC00**

Note that the total capacitance for the switching output must be measured under open-socket conditions for accurate calculations. Considering these conditions, the data sheet $C_{pd}$ is calculated using equation 11. Due to the automatic test-equipment constraints, $C_{pd}$ is not assigned a maximum value in the data sheet.

$$C_{pd} = \frac{I_{CC}}{V_{CC} \times f_I} - C_{L(eff)} \quad (11)$$

Where:

$f_I$ = input frequency (Hz)
$V_{CC}$ = supply voltage (V)
$C_{L(eff)}$ = effective load capacitance on the board (F)
$I_{CC}$ = measured value of current into the device (A)

The effective load capacitance is calculated according to equation 12 (assuming $C_L$ is equal in all outputs).

$$C_{L(eff)} = C_L \times N_{SW} \times \frac{f_O}{f_I} \quad (12)$$

Where:

$f_O/f_I$ = ratio of output and input frequency (Hz)
$N_{SW}$ = number of bits switching
$C_L$ = load capacitance (F)

To explain the $C_{pd}$ and the method of calculating dynamic power, see Table 1, which gives the $C_{pd}$ test conditions for AHC devices. The symbols used in Table 1 for $C_{pd}$ of AHC devices are:

V = $V_{CC}$ (5 V)
G = ground (GND) (0 V)
1 = high logic level = $V_{CC}$ (5 V)
0 = low logic level = ground (0 V)
X = irrelevant: 1 or 0, but not switching
C = 50% duty cycle input pulse (1 MHz), (see Figure 6)
D = 50% duty cycle input (1/2 frequency) out-of-phase input pulse (see Figure 6)
S = standard ac output load (50 pF to GND)

The table shows the switching of each pin for AHC devices. Once the $C_{pd}$ is determined from the table, the $P_D$ is easy to calculate using equations 8 and 9.

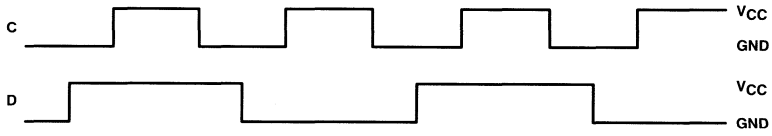



**Figure 6. Input Waveform**

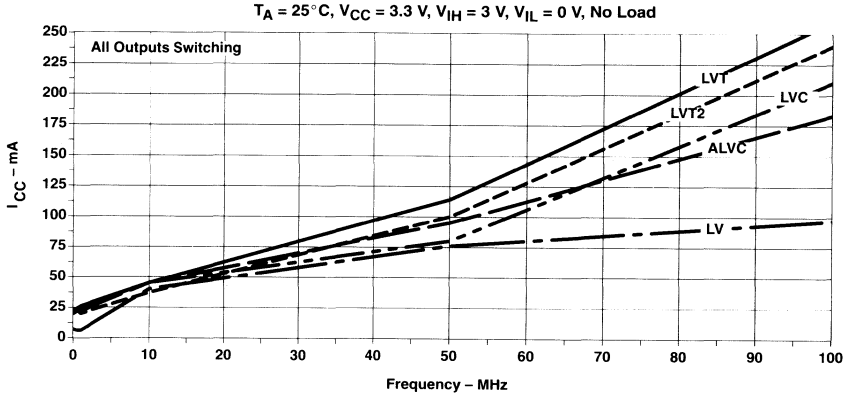
**Table 1. $C_{pd}$ Test Conditions With One- or Multiple-Bit Switching**

| TYPE | PIN | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
| AHC00 | C | 1 | S | X | X | S | G | S | X | X | S | X | X | V | | | | | | |
| AHC02 | S | C | 0 | S | X | X | G | X | X | S | X | X | S | V | | | | | | |
| AHC04 | C | S | X | S | X | S | G | S | X | S | X | S | X | V | | | | | | |
| AHC08 | C | 1 | S | X | X | S | G | S | X | X | S | X | X | V | | | | | | |
| AHC10 | C | 1 | X | X | X | S | G | S | X | X | X | S | 1 | V | | | | | | |
| AHC11 | C | 1 | X | X | X | S | G | S | X | X | X | S | 1 | V | | | | | | |
| AHC14 | C | S | X | S | X | S | G | S | X | S | X | S | X | V | | | | | | |
| AHC32 | C | 1 | S | X | X | S | G | S | X | X | S | X | X | V | | | | | | |
| AHC74 | 1 | D | C | 1 | S | S | G | S | S | X | X | X | 1 | V | | | | | | |
| AHC86 | C | 1 | S | X | X | S | G | S | X | X | S | X | X | V | | | | | | |
| AHC138 | C | 0 | 0 | 0 | 0 | 1 | S | G | S | S | S | S | S | S | S | V | | | | |
| AHC139 | 0 | C | 0 | S | S | S | S | G | S | S | S | S | X | X | X | V | | | | |
| AHC240 | 0 | C | S | X | S | X | S | X | S | G | X | S | X | S | X | S | X | S | X | V |
| AHC244 | 0 | C | S | X | S | X | S | X | S | G | X | S | X | S | X | S | X | S | X | V |
| AHC245 | 1 | C | X | X | X | X | X | X | X | G | S | S | S | S | S | S | S | S | 0 | V |
| AHC373† | 0 | S | D | D | S | S | D | D | S | G | C | S | D | D | S | S | D | D | S | V |
| AHC374‡ | 0 | S | D | D | S | S | D | D | S | G | C | S | D | D | S | S | D | D | S | V |
| AHC540 | 0 | C | X | X | X | X | X | X | X | G | S | S | S | S | S | S | S | S | 0 | V |
| AHC541 | 0 | C | X | X | X | X | X | X | X | G | S | S | S | S | S | S | S | S | 0 | V |
| AHC573† | 0 | D | D | D | D | D | D | D | D | G | C | S | S | S | S | S | S | S | S | V |
| AHC574‡ | 0 | D | D | D | D | D | D | D | D | G | C | S | S | S | S | S | S | S | S | V |

† All bits switchings, but with no active clock signal
‡ All bits switching

## Comparison of Supply Current Versus Frequency

$C_{pd}$ and dynamic power consumption can be measured through supply-current-versus-frequency plots. Supply current is critical because it indicates the amount of power consumed by the device. A small value for $I_{CC}$ is desirable because reducing the amount of power consumed yields many benefits. Less power consumed means less heat is generated and the problems of dissipating the heat are reduced. The reliability of a system is also improved, because lower stress gradients are present on the device and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. Figures 7 and 8 illustrate $I_{CC}$ versus frequency data for TI's '245 device in different families for both 5 V and 3.3 V.



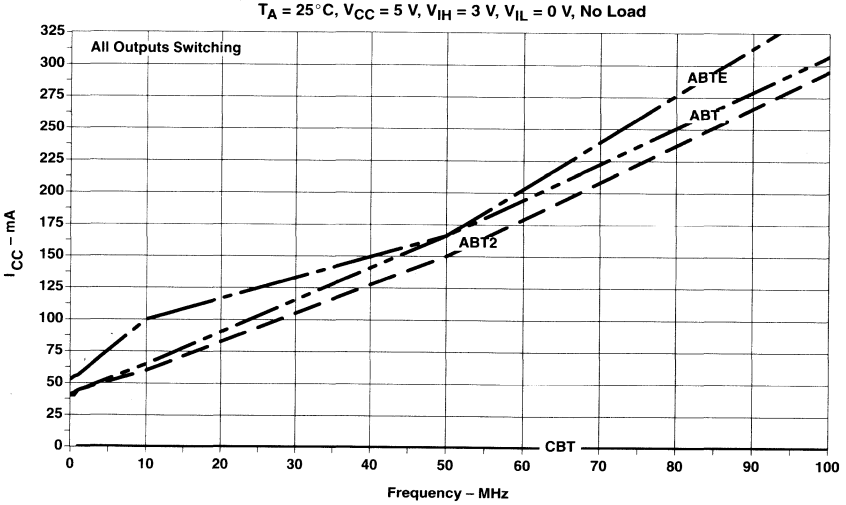




**Figure 7. Power Consumption With All Outputs Switching**

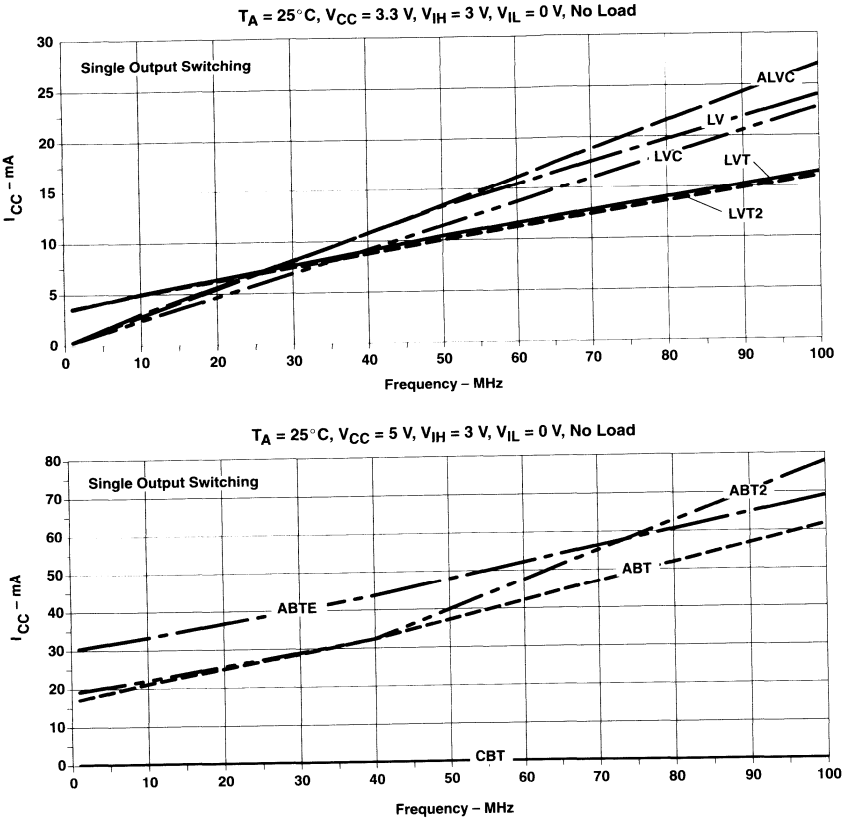



**Figure 8. Power Consumption With a Single Output Switching**

## Power Economy

As noted previously, the industry trend has been to make devices more robust and faster while reducing their size and power consumption. This section describes the rationale and methods used to minimize power consumption in a CMOS circuit. For a CMOS system design, each module is allocated a fixed power budget. This is a power consumption that the module must not exceed. It is important to meet this power consumption allocation constraint, along with other constraints, to achieve a balanced design.

Power consumption minimization can be achieved in a number of ways. The dc power consumption can be reduced to leakage by using only CMOS logic gates, as opposed to bipolar and BiCMOS. The leakage, in turn, is proportional to the area of diffusion, so the use of minimum-size devices is an advantage. One of the system design considerations is the choice of low-power devices, with systems today using devices in the 1.5-V to 3.3-V $V_{CC}$ range. Dynamic power consumption can be limited by reducing supply voltage, switched capacitance, and frequency at which the logic is clocked.

Consider TI's low-power CMOS devices, such as advanced low-voltage CMOS (ALVC) technology as an example. ALVC is the highest-performance 3.3-V bus-interface family. These specially designed 3-V products are processed in 0.6-µm CMOS technology, giving typical propagation delays of less than 3 ns, along with a current drive of 24 mA. This low supply voltage reduces both static and dynamic power consumption for the ALVC family. ALVC also has ultra-low standby power.

## Conclusion

Power consumption is a function of load capacitance, frequency of operation, and supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heatsinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower-temperature stress gradients on the device. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.


## Acknowledgment

The author of this application report is Abul Sarwar.

# *Designing With Logic*

SDYA009C
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TEXAS INSTRUMENTS

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## Abstract

Data sheets, which usually give information on device behavior only under recommended operating conditions, may only partially answer engineering questions that arise during the development of systems using logic devices. However, information is frequently needed regarding the behavior of the device outside the conditions in the data sheet. Such questions might be: "How does a bus driver behave with reduced (or even switched-off) supply voltage?" or "How does the delay time of a gate with a large capacitive load change?" or "What must be considered when using *backdriving*?".

This report gives information on a number of questions that frequently arise. In addition, it provides examples that explain phenomena that the designer should be aware of when using devices outside their recommended operating conditions.


## 1 Introduction

The function and behavior of digital logic devices are described fully in data sheets. Most questions regarding the behavior of the device that arise when developing a system can be answered with the information given. However, the devices might be operated under conditions not covered by the data sheet. This report addresses this issue and provides information on the behavior of devices under such conditions.

Many parameter values in data sheets are not measured when the circuits are tested. The information is based on typical values that have been established experimentally and that are applicable to the majority of devices of the same type or family. In individual cases it might be necessary to interpret data and make measurements to accurately forecast the behavior of the complete system.

## 2 Behavior With the Supply Voltage Reduced

Although not specifically mentioned in data sheets, additional components, some of them parasitic, influence operational characteristics of devices. These components can affect the function of a system if the devices are not operated within the recommended operating conditions. For example, large systems often require that parts of the system be shut down while other parts continue to operate. Frequent problems occur at the interfaces between subsystems, which are operated with different supply voltages, or whose supply voltages are switched off. This section describes the behavior of digital circuits operated with low supply voltages.

### 2.1 Behavior With the Supply Voltage Switched Off

Because many circuits can be used with the various logic families, no general rule applies to the behavior of systems with supply voltages switched off. For this reason, only the most important circuits and their behavior are discussed.

#### *2.1.1 Bipolar Circuits*

Figure 1 shows the simplified circuit of a TTL device with diode inputs, such as are used with devices in the SN74LS (low-power Schottky TTL) logic family. However, the following comments apply to all other bipolar logic families.

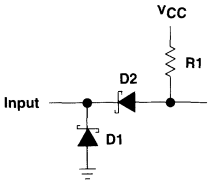


**Figure 1. Input Circuit of a Bipolar Device**

When the supply voltage in a system is switched off ($V_{CC}$ = 0 V), the $V_{CC}$ pin of a logic device is short circuited to ground via the other components in the system. If a voltage is then applied to the input of a device, as shown in Figure 1, and if this voltage lies within the logic-level range ($V_I$ = 0 to 5.5 V), diode D2 is blocking and the clamping diode D1 is biased into a blocking state. Therefore, a very small current flows into the device, corresponding to the leakage current of these diodes. The value for this current given in the data sheets for the corresponding input voltage can be used. This statement applies, without exception, to all TTL devices.

Figure 2 shows the output stage of circuits from the SN74 (standard TTL) series. Parasitic collector-substrate diode D2 and diode D3 are in a blocking position between the $V_{CC}$ and GND connections of all devices. If the $V_{CC}$ pin is at GND potential and a positive voltage is applied to the output, diode D1 is blocking and the output is in the high-impedance state.

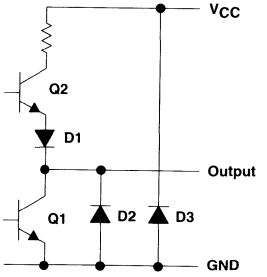


**Figure 2. Device Output From SN74 Family (Standard TTL)**

Other bias relationships result when supply voltages are switched off to Schottky TTL devices (SN74LS, SN74S, SN74ALS, SN74AS, and SN74F series). Figure 3 shows the important parts of the output stage. If a voltage is applied to the output of the device whose supply voltage is switched off, parasitic diode D1, which is in parallel with resistor R, becomes conductive. The output is then at a low impedance.

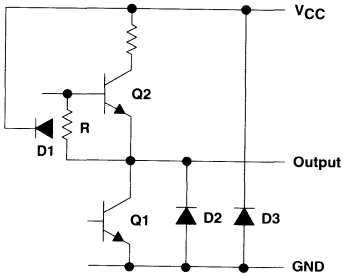


**Figure 3. Output of Schottky TTL Devices**

If the circuit in Figure 3 is modified for bipolar devices using 3-state outputs, parasitic diode D1 at the output is no longer significant. One possibility is to tie resistor R to GND potential instead of to the output of the circuit (see Figure 4). In this case, the output remains at a high impedance when the supply voltage is switched off.

The outputs of TTL circuits with an open collector are always at a high impedance when the supply voltage is switched off.

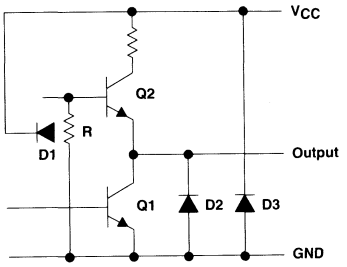


**Figure 4. 3-State Output of Schottky TTL Devices**

### *2.1.2 CMOS Circuits*

The behavior of CMOS devices when the supply voltage is switched off is essentially determined by the protective circuits at the inputs and outputs. These circuits are intended to protect the device from damage from electrostatic discharge (ESD). Figure 5 shows, in simplified form, the construction of a CMOS circuit with additional diode paths at the input and output. Both the input, via diode D1, and the output, via diode D3, are at a low impedance when the supply voltage is switched off. Diode D3 also exists in circuits having an open drain at the output.

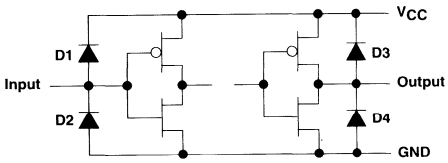


**Figure 5. Diode Paths in CMOS Devices**

## 2.2 Behavior With Low Supply Voltages

The behavior of logic devices at low supply voltages is difficult to predict because a detailed knowledge of the internal circuit, including its dimensions, is necessary. An example is the behavior of a noninverting buffer with open-collector outputs (SN7407) when the supply voltage is switched on and off. Figure 6 shows the internal circuit of the SN7407. At supply voltages lower than the forward voltage of the diode path (base-emitter path), all transistors are blocking. Therefore, the output voltage ($V_O$) first follows the supply voltage ($V_{CC}$). When the latter reaches about 0.7 V, current flows via resistor R3 into the base of transistor Q4 and the output switches to a low level. If the supply voltage reaches a value of $3 \times V_{be}$, and if a logic high is applied to the input, current flows into the base of transistor Q3 (via transistors Q1 and Q2), which switches. Output transistor Q4 is again switched off, causing the output voltage to rise to the value of $V_{CC}$. In the previous analysis, the voltage drop necessary for a sufficient base current to switch on the transistor is neglected. TTL devices attain stability with a supply voltage of about 3.5 V, and are fully functional at a typical voltage of 4 V. However, with supply voltages below the minimum specified in data sheets, not all parameters can be attained. This applies to both dc parameters, such as output currents and voltages, and to switching characteristics, such as propagation delay time and maximum clock frequency.

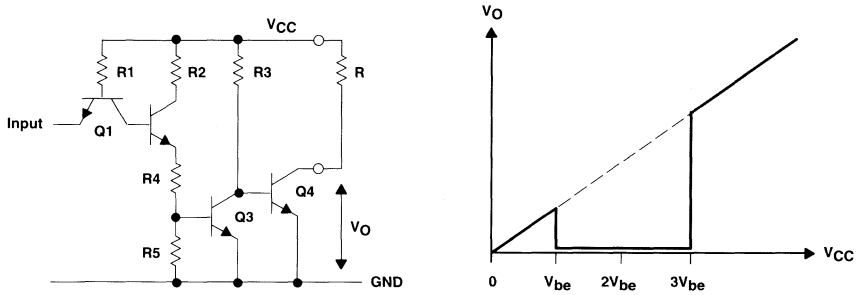


**Figure 6. Behavior of a TTL Device at Low Supply Voltages**

In a manner similar to TTL devices, CMOS devices also fail to operate at supply voltages below the threshold voltages of the MOS transistors. If the supply voltage is further increased, parts of the circuit are activated (see Figure 6). As previously mentioned, the precise circuit configuration of the device determines the circuit behavior. Full functionality of CMOS devices from the SN74HC family is ensured from $V_{CC}$ = 2 V, whereas the 74AC family can be ensured only from 3 V, although the latter is also stable, with a supply voltage of only 2 V. Since the maximum clock frequency of CMOS devices is dependent on the supply voltage, at a high clock frequency, circuits might not operate reliably during the switch-on or switch-off phases, even though the supply voltage is more than 2 V.

Special design measures have been taken to achieve a defined behavior, even when circuits are operated at supply voltages far below the conditions recommended in data sheets. For example, on bus drivers of the BiCMOS series (SN74ABT/BCT), a voltage-monitoring circuit ensures that the 3-state outputs remain in the high-impedance state at supply voltages below about 3.5 V, regardless of the inputs to these devices. At supply voltages above this threshold voltage, the control inputs (enable and disable) are effective. If a voltage level is applied to these inputs that results in a high impedance at the output, the same state is implemented at the output.

## 2.3 Supply Voltages Partially Switched Off

In large systems, often part of the voltage supply is switched off, while other parts of the system continue to operate. Then, the critical part of the system is the interface between the device that is supplied and the device that is not supplied with voltage. In such a case, two requirements must be met. First, the part of the system that continues to operate must not be disturbed by the part that is switched off. Second, the switched-off part must not be disturbed by voltages fed back from the operating part.

These requirements can be met with bipolar circuits. As mentioned previously, the inputs of switched-off bipolar circuits are at a high impedance and do not influence parts of the device that are still active. With outputs of switched-off parts of devices that are connected to active parts, only the outputs of bus drivers (e.g., SN74xx240 or SN74xx245) are at a high impedance. Therefore, only such devices should be used for bus lines connecting systems. For unidirectional lines that connect switched-off and active devices, it must be determined in each case whether the operation of the system could be influenced by the outputs being at a low impedance when switched off. If this is not the case, then at this position in the system, any kind of device, including CMOS, can be used.

As mentioned previously, when switching the supply on and off, the logic state of the devices concerned cannot be ensured. Therefore, undefined states can arise during this time at the interfaces and cause malfunction of the system (see Figure 6). The use of SN74ABT/BCT-series bus drivers provides a solution, since the outputs of these parts go into the high-impedance inactive state at supply voltages below about 3.5 V. A difficult situation arises when using CMOS devices. As shown in Figure 5, these parts have protective diodes that are connected to the supply rails at both inputs and outputs. If the supply voltage $V_{CC2}$ of this circuit is switched off (see Figure 7) while the supply voltage $V_{CC1}$ remains switched on, a current (I) flows out of gate G1, via diode D1, into the next circuit. This current can rapidly overload protective diode D1 (the maximum current of the input clamp diodes of CMOS devices is only 20 mA) and destroy the device. Remember that, in general, the next device represents a short circuit and, apart from the output resistance of gate G1, there is no current-limiting circuit element.

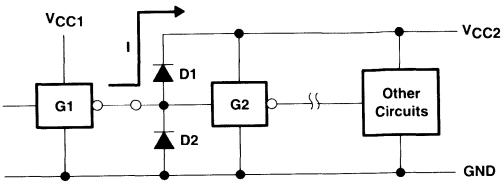


**Figure 7. Feeding Back With CMOS Devices**

Figure 8 shows recommended design ideas, with reservations, to provide some current limiting. In Figure 8a, the input current of the switched-off device is limited by resistor R. Using this, the input current of the circuit to be protected can be limited to a permissible value. The input current of CMOS devices is extremely low and series resistors of several ohms usually have no negative effect on the function of the part. However, feeding of the next device, via input clamping diode D1, is not prevented entirely.

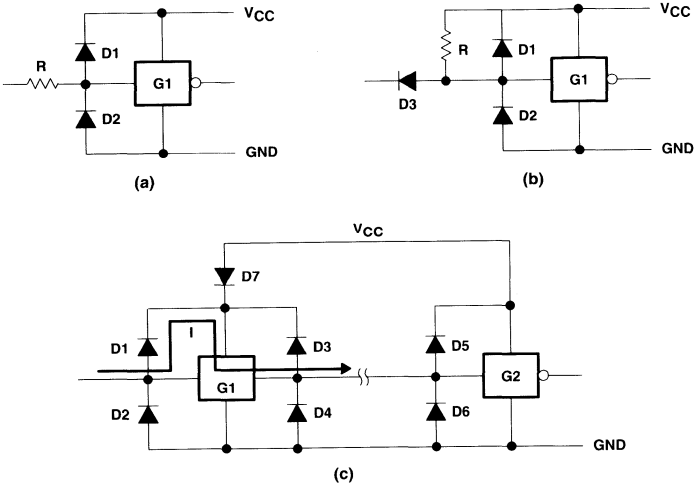


**Figure 8. Ideas for Protecting CMOS Devices**

In the circuit of Figure 8b, the flow of current into the device to be protected when the supply voltage $V_{CC}$ is switched off, is prevented by diode D3. However, to ensure a high level at the input of gate G1 with normal operation, a pullup resistor is needed, and this significantly increases the power consumption of the CMOS circuit. D3 also shifts the logic level at the input of the gate, and as a result, reduces the noise margin of the circuit. Apart from the noise-margin restriction, this circuit is effective, because it prevents feedback into the switched-off part of the device.

The diode in Figure 8c has no effect if gate G1 has a noninverting function. Even so, the flow of current via clamping diode D1 and the $V_{CC}$ rail of gate G1 into the next circuit is prevented. Instead, the current flows via the output of gate G1, which, in this case, is at a high logic level, and into the following circuit.

### 2.4 Changing Powered-Up Subsystems

In many applications, to carry out service or repair work without interrupting operation, it must be possible to change individual subsystems. Because of the partial switch off of supply voltage described previously, this is permissible only when circuit design modifications are made that prevent the destruction of semiconductor components and ensure that the operation of the rest of the system is not disturbed.

In the input and output circuits of logic devices, some desired and some parasitic diodes are present. As explained, these components represent additional current paths, and undefined currents may flow into the device, either through the clamping diodes to the inputs and outputs, or through additional parasitic diodes in the devices. To avoid uncontrolled operational states, changing powered-up subsystems is permissible only if the subsystems have a leading GND pin as a reference potential.

If the connection of the GND reference potential is made first when inserting subsystems, and broken only after removing them, the operational state that results when changing subsystems can be limited to the cases previously mentioned. This assumes that parts of the system that have the same reference potential are not supplied with voltage.

The inputs of bipolar logic circuits, including devices in the SN74ABT/BCT series that are in subsystems to be changed, are at a high impedance under all conditions and, therefore, no problems should be expected. The totem-pole outputs of most TTL devices are at a low resistance when the supply voltage is switched off, so when reinserting a subsystem, the line concerned is switched to low, which may be incorrect. Three-state outputs of bipolar devices are at a high impedance when the supply voltage is switched off. However, they can go to a low impedance for a short time during switch on or switch off. This could generate an incorrect logic level because at low supply voltages the internal circuit does not operate properly. The result is that during the change of subsystems, short-duration undefined signals that disturb other systems may appear at the corresponding outputs. This problem can be avoided if devices from the SN74ABT/BCT series are used. With these components, the outputs are switched into the inactive high-impedance state if the supply voltage falls below about 3 V.

The problem of changing subsystems with power supplied can be easily solved, particularly when using devices that include a supply-voltage monitor, but CMOS circuits can be used only under these circumstances with certain restrictions. In this case too, the use of a leading GND pin on the connector is essential. The CMOS inputs of devices on the subsystem to be changed should, in every case, be protected at least with series resistors (see Figure 8a), to prevent excessive currents in the clamping diodes of the input protection circuitry. In extreme cases, depending on the layout of pins on the connector, the current for the complete subsystem could, for a short time, flow through one of these diodes. For the outputs of CMOS devices, no practicable protection circuit can be recommended. Also, the use of protective resistors must be considered to limit the current in the clamping diodes at the output. However, this is not possible in most cases because an unacceptable reduction in the output drive capability would result.

## 3 Unused Inputs

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used. Such parts should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. A rule that must be observed under all circumstances is:

> All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.

The logic level that should be applied to any particular unused input depends on the function of the device. As a result of the input circuits of bipolar devices, a high level is established at open-circuited inputs. The voltage at such an input corresponds to the threshold voltage of the input circuit (about 1.4 V or 1.1 V with devices from the SN74LS family). In a test of the function of such a circuit, this order of voltage at the input, in general, indicates that this circuit is open. CMOS inputs are of such high impedance that the smallest change on the open input can generate any undesired logic level. A slight change of the capacitance at the unconnected input, for example, by bringing the hand close to the package, can so change the effective voltage at the input that a high level can change into a low level, or vice versa. Additionally, for the same reasons mentioned, unconnected inputs may react to all kinds of coupled-in interference voltages, and the behavior of the circuit can no longer be predicted.

With gates, another solution is to connect unused inputs to an input of the same gate that is in use. The function of the device is unaffected. This circuit arrangement can be used equally well with AND (NAND) as with OR (NOR) gates (see Figure 9). Here, connecting the inputs together increases the capacitive load on the driver stage and, with bipolar circuits, also increases the dc current drain.


**Figure 9. Interconnection of Unused Inputs With AND and OR Gates**

In many cases, the simple method shown here cannot be used, especially if the unused inputs are not part of the same gate function. In this case, a defined logic level must be applied to the unused inputs. If a low level is required, the input should be directly connected to GND; if a high level is required, it should be connected with a voltage source corresponding with a high level. In general, this is the positive supply voltage $V_{CC}$. Figure 10 shows how, in the previously mentioned cases, a fixed potential should be connected to unused inputs. Note that a high level should be applied to the unused inputs of an AND (NAND) function and a low level to unused inputs of an OR (NOR) function.

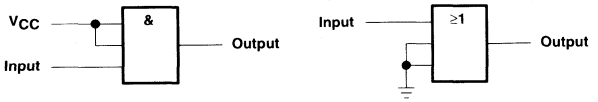


**Figure 10. Fixed Potential Connected to Unused Inputs**

Devices with multiple-emitter inputs (SN74 and SN74S series) are exceptions. Since no voltage greater than 5.5 V should be applied to the inputs (because if exceeded, the base-emitter junction at the inputs breaks down), the inputs of these devices must be connected to the supply voltage $V_{CC}$ via series resistor $R_S$ (see Figure 11). This resistor should be dimensioned such that the current flowing into the gate or gates, which results from overvoltage, does not exceed 1 mA. But, because the high-level input current of the circuits connected to the gate flows through this resistor, the resistor should be dimensioned so that the voltage drop across it still allows the required high level. Equations 1 and 2 are for dimensioning resistor $R_S$, and several inputs can be connected to a high level via a single resistor if the following conditions are met:

$$R_{S(min)} = \frac{V_{CCP} - 5.5\ V}{1\ mA} \quad (1)$$

$$R_{S(max)} = \frac{V_{CC(min)} - 2.4\ V}{n \times I_{IH}} \quad (2)$$

Where:

n = number of inputs connected
$I_{IH}$ = high input current (typical 40 µA)
$V_{CC(min)}$ = minimum supply voltage $V_{CC}$
$V_{CCP}$ = maximum peak voltage of the supply voltage $V_{CC}$ (about 7 V)

If part of a device is unused, the unused-input rules should be applied. If, for example, in an application only one flip-flop from a dual flip-flop type SN74ALS74 is used, all inputs of the unused flip-flop should be connected to a defined logic level, which, in this case, could be either low or high.

**NOTE:**
Unused outputs of a device should not be left unconnected (open).

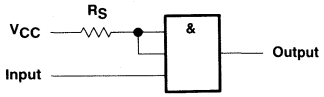


**Figure 11. Series Resistor Connected to Unused Inputs of Multiple-Emitter Transistors**

## 4 Excessive Input Currents

All logic devices have protection circuits at outside connections. These diodes, or similar components, are intended to protect the device against destruction by ESD. In addition, clamping diodes at device inputs limit overvoltage and undervoltage resulting from line reflections and divert the currents that flow, in consequence, to either the negative (GND) or positive ($V_{CC}$) supply rails. Currents that flow in these circuit parts can, under certain circumstances, activate so-called parasitic transistors, which results in incorrect operation of the circuit.

Examples of this are the clamping diodes at the inputs of HCMOS devices, which are intended to limit overvoltages resulting from reflections. These diodes are created with a P-doped region in an N-doped substrate which, in turn, is connected to the positive supply voltage (see Figure 12). Between two adjacent diodes and in conjunction with the substrate, a parasitic PNP transistor is effectively created. A part of the current in one of the two clamping diodes is, therefore, not diverted to the $V_{CC}$ rail but, instead, flows to an adjacent input. The current gain of this transistor is small (about 0.01), so that under normal operating conditions no effect can be expected. If, however, a high positive voltage is applied to the input of a circuit, as in Figure 12, which adapts signal voltages with an amplitude of 24 V to HCMOS circuits, a current flows into the adjacent input, despite the low current gain of the parasitic transistors. The current in the adjacent input may then be sufficient to generate a false input signal. However, destruction or damage to the device (as a result of latch-up) is not likely to occur.

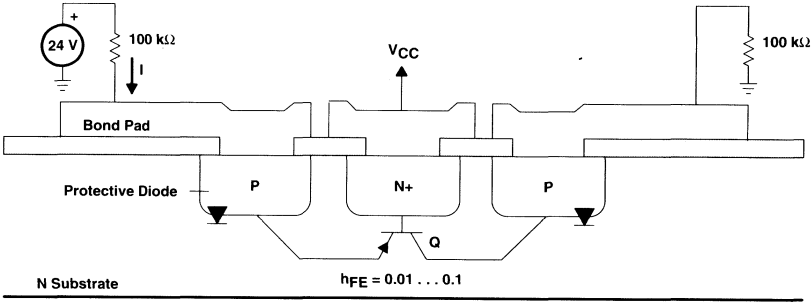


**Figure 12. Parasitic Transistors in CMOS Input Stages**

Similar effects caused by parasitic transistors also can be observed with bipolar transistors. Figure 13 shows a bipolar input that includes Schottky clamping diodes, realized with an N-doped region covered by a metallic contact. With a small negative input current, the forward voltage of the Schottky diode is about 400 mV, and the current in such an input is diverted, via the diode, to the GND pin of the device. If this current is increased, the forward voltage of the diode increases accordingly, and at a certain amplitude exceeds 700 mV. At this point, the silicon diode (which results from the N-doped region and the P-doped substrate under it, connected to the GND of the device) conducts. Here, also, a parasitic transistor is activated, whereby the whole adjacent N-doped region, comprising the collectors of active transistors, functions as a collector. This collects together a part of the current circulating in the substrate. If the amplitude of the negative current is sufficient, incorrect operation of the circuit can be expected.

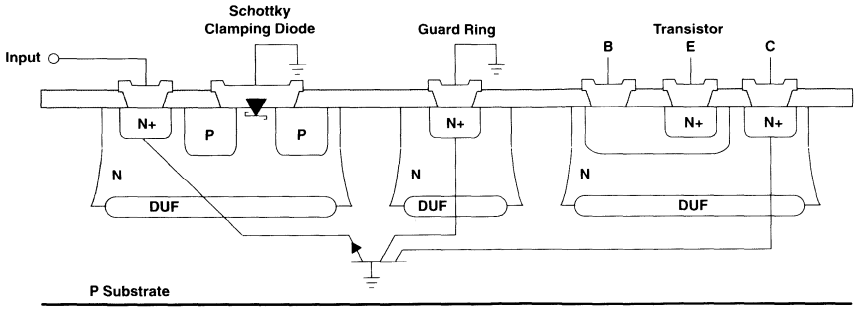


**Figure 13. Parasitic Transistors in Bipolar Input Circuits**

Negative voltage undershoot of considerable amplitude must be expected in practical operation of logic devices. Therefore, the semiconductor manufacturer must take the steps necessary to ensure reliable operation. Guard rings, which are placed in a ring around the circuit in question (see Figure 13), ensure reliable operation. In this example, these guard rings consist of an N-doped region connected to GND potential, which has the effect of an additional collector for the parasitic transistors, collecting the majority of the current circulating in the substrate and diverting it to GND potential. These guard rings are constructed so that a negative input current of $I_{IN}$ = –60 mA with a duration t = 100 ns does not cause an incorrect function of the circuit. These values are again reflected in Figure 14. Here, a TTL device with a signal amplitude of 3 V drives a 10-meter-long coaxial cable with a characteristic impedance of Z = 50 Ω at the end of which the input circuitry (with clamping diode) of the device in question is connected. High-amplitude current pulses, such as those generated by line reflection, are captured with this measuring setup.

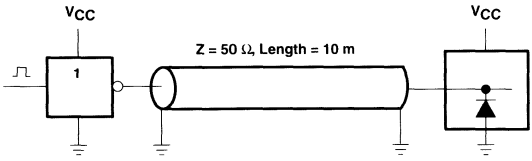


**Figure 14. Setup for Generating an Undershoot Pulse (I = –60 mA, t = 100 ns)**

Negative input currents with an amplitude of only a few milliamperes, but with a duration of several microseconds, can cause incorrect operation of the device. Since the transit frequency of the parasitic transistors is only about 1 MHz, the circuit and dimensioning of guard rings are simplified. A certain duration of the undershoot pulse is necessary to switch on the parasitic transistors, and possibly to cause abnormal operation of the circuit.

## 5 Transition Times

Correct operation of the circuit can be ensured only if the rise and fall times of the signal at the input do not exceed certain values. With CMOS devices (SN74HC and 74AC/SN74AC), these values are given in the data sheets. For devices from the SN74HC series, a rise and fall time (transition time) less than 500 ns is specified at $V_{CC}$ = 4.5 V, while for ACL devices (74AC/SN74AC series), a value of 10 ns/V is given. Figure 15 shows this in more detail.

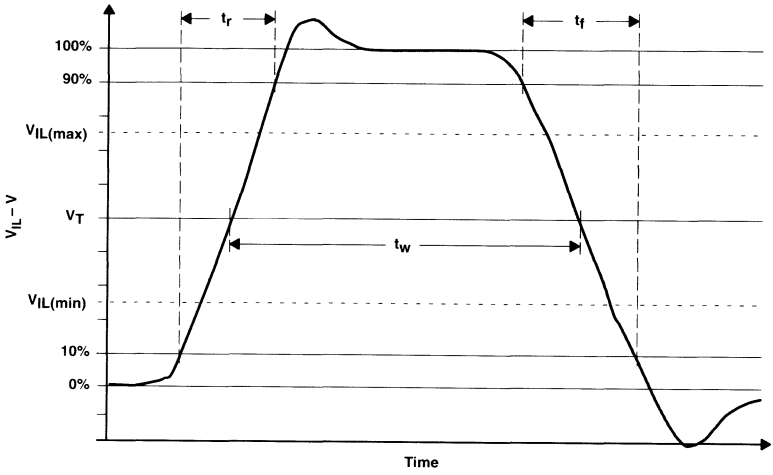


**Figure 15. Definition of Signal Amplitude and Pulse Width**

The signal amplitude is specified as the difference between the two stable signal levels for high ($V_H$) and low ($V_L$); overshoot and undershoot of the signal are not taken into account. The difference $V_H - V_L$ is taken as 100% of the amplitude. The rise time of the signal is defined as the time taken to rise from 10% to 90% of the full amplitude; similarly, the fall time is the time taken to fall from 90% to 10% of the amplitude. The pulse width ($t_w$) of a signal is measured at 50% of the amplitude. However, these definitions must be used for digital circuits with certain qualifications because, in most cases, the switching threshold ($V_T$) of the input is not 50% of the amplitude. So, the level needed by the circuit must be considered and, from this, the required signal waveform derived.

The values of voltage that are decisive for the correct operation of the part are the maximum permissible low voltage at the input $V_{IL(max)}$ and the minimum necessary high voltage at the input $V_{IH(min)}$. The following example applies for a device from the SN74HC series:

$V_{IL(max)} = 0.9$ V

$V_{IH(min)} = 3.15$ V at $V_{CC} = 4.5$ V

However, the rise and fall times are specified between 10% ($0.1 \times V_{CC} = 0.45$ V) and 90% ($0.9 \times V_{CC} = 4.05$ V) of the amplitude. The voltage waveform below 0.9 V (low level) and above 3.15 V (high level) has no influence on the function of the device, as long as the absolute maximum ratings are not exceeded. Therefore, it is better to define rise and fall times over the range between $V_{IL(max)}$ and $V_{IH(min)}$, which must be adhered to in order to ensure correct functioning of the device. From the amplitude (4.5 V) and the rise time specified in the data sheet ($t_r$ = 400 ns), the transition time (dt/dv) rate can be derived as follows:

$$dv/dt = \frac{400 \text{ ns}}{(0.9 \times V_{CC}) - (0.1 \times V_{CC})} = \frac{400 \text{ ns}}{3.6 \text{ V}} = 110 \text{ ns/V} \quad (3)$$

The input signal must cross the region between $V_{IL(max)}$ and $V_{IH(min)}$ (and vice versa) at the transition rate or faster. This value is comparable to the transition rate given in 74AC-series data sheets of dt/dv = 10 ns/V. The pulse width ($t_w$) is measured at the actual threshold voltage ($V_T$) of the circuit and with CMOS devices at 50% of the amplitude. Bipolar and TTL-compatible CMOS devices have a switching threshold that is shifted considerably from the middle of the signal amplitude. This shift must then be taken into account when determining the pulse width. Table 1 shows the necessary minimum transition rise/fall rates for various logic families.

**Table 1. Required Minimum Input Rise/Fall Rates for Logic Families**

| SERIES | $V_{CC}$ (V) | $V_{IL(max)}$ (V) | $V_{IH(min)}$ (V) | $V_T$ (V) | dt/dv (ns/V) |
|---|---|---|---|---|---|
| SN74 | 4.75–5.25 | 0.8 | 2 | 1.4 | 15 |
| SN74LS | 4.75–5.25 | 0.8 | 2 | 1.4 | 15 |
| SN74S | 4.75–5.25 | 0.8 | 2 | 1.4 | 15 |
| SN74ALS | 4.5–5.5 | 0.8 | 2 | 1.4 | 15 |
| SN74AS | 4.5–5.5 | 0.8 | 2 | 1.4 | 15 |
| SN74F | 4.5–5.5 | 0.8 | 2 | 1.4 | 15 |
| SN74HC | 2 | 0.3 | 1.5 | 1.4 | 625 |
| | 4.6 | 0.9 | 3.15 | 2.25 | 110 |
| | 6 | 1.2 | 4.2 | 3 | 80 |
| SN74HCT | 4.5–5.5 | 0.8 | 2 | 1.4 | 125 |
| 74AC | 3 | 0.9 | 2.1 | 1.5 | 10 |
| | 4.5 | 1.35 | 3.15 | 2.25 | 10 |
| | 5.5 | 1.65 | 3.85 | 2.75 | 10 |
| 74ACT | 4.5–5.5 | 0.8 | 2 | 1.4 | 10 |
| SN74BCT | 4.5–5.5 | 0.8 | 2 | 1.4 | 10 |
| SN74ABT | 4.5–5.5 | 0.8 | 2 | 1.4 | 5/10 |
| SN74LV | 2.7–3.6 | 0.8 | 2 | ≈1.5 | 100 |
| SN74LVC | 2.7–3.6 | 0.8 | 2 | ≈1.5 | 5/10 |
| SN74LVT | 3.0–3.6 | 0.8 | 2 | 1.4 | 10 |

The values for the transition rise/fall rates (dt/dv) are understood to be a level that ensures the function of individual components if the circuit is controlled with these rates. This does not necessarily mean that the device operates correctly under all circumstances in a large system. Figure 16 shows this in more detail. It shows two D-type flip-flops connected as a two-stage shift register. The first flip-flop is the TTL-compatible device 74ACT11074 (input threshold voltage = 1.5 V), but the second flip-flop (74AC11074) has CMOS-compatible inputs with an input threshold voltage of $0.5 \times V_{CC}$.

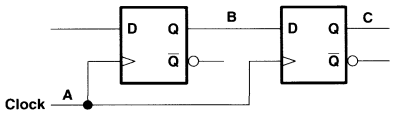


**Figure 16. Two-Stage Shift Register**

According to Table 1, devices from the 74ACT series must be controlled with a transition rate of at least 10 ns/V, if the function of individual parts is to be ensured. If, however, the behavior with time of the circuit is analyzed, it is found that the shift register does not behave as required (see Figure 17). When the clock signal reaches 1.5 V (having the required transition rate of 10 ns/V), the first flip-flop switches. The output typically reacts about 5 ns later. Only after another 5 ns does the voltage of the clock signal reach a value of 2.5 V, so that the second flip-flop switches. As a result of this late triggering, it accepts incorrect information: namely, the state that the first flip-flop has reached after the switching clock edge, and not the state that the flip-flop had before the clock edge.

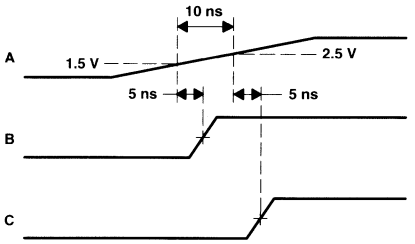


**Figure 17. Incorrect Operation of a Shift Register**

Under typical operating conditions, the circuitry would, however, operate correctly. The output signals of advanced CMOS devices have a rise time <5 ns (typical 2 ns). At the clock signal, a voltage change of 1.5 V to 2.5 V takes place in about 1.25 ns. A 74ACT11074 flip-flop has a minimum delay time of 1.5 ns, and under these circumstances correct functioning of the circuit is ensured.

Similarly, problems need not be expected when using devices from other families under similar conditions, as long as the signals have nominal rise and fall times. Under extreme conditions (for example, with unfavorable line routing), the switching times can be so lengthened that faults of the kind just described may occur.

## 6 Propagation Delay Times

### 6.1 Propagation Delay Times With Several Outputs Switching Simultaneously

The propagation delay times of circuits given in data sheets apply when only one output switches at a time. The reason for this is that the production equipment used to test circuits can test only one transmission channel at a time. If several outputs switch simultaneously, the propagation delay times given in data sheets can be used only with reservations. The reason for this is that the package inductances ($L_P$) of the supply-voltage lines, as well the output lines (see Figure 18), have a significant influence on the circuits and, thus, on the delay times. These inductances have the effect that the current in the power supply lines, and consequently in the output of the device, has a limited rate of rise. For this reason, when several outputs switch simultaneously, only a limited output current is available.

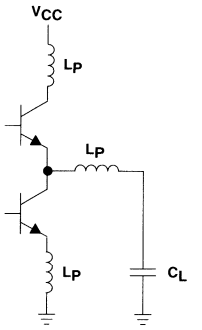


**Figure 18. Inductances in the Lines Supplying a Package**

Figure 19 shows the influence on the delay time of the number of outputs that are switched simultaneously. When packages having two supply-voltage pins ($V_{CC}$ and GND) are used, as is the case with the majority of digital logic devices, an increase of the delay time of 150 ps to 200 ps for each additional output that is simultaneously switched must be expected. With an octal bus driver, such as an SN74xx240, the delay time is increased by 1 ns to 1.4 ns when all eight outputs switch simultaneously. In those cases where there are several supply-voltage pins, such as the advanced CMOS devices in the 74ACT series from Texas Instruments (TI), the result influences speed of the circuit. As shown in Figure 19, the loss of speed of the components is halved when several outputs switch simultaneously.

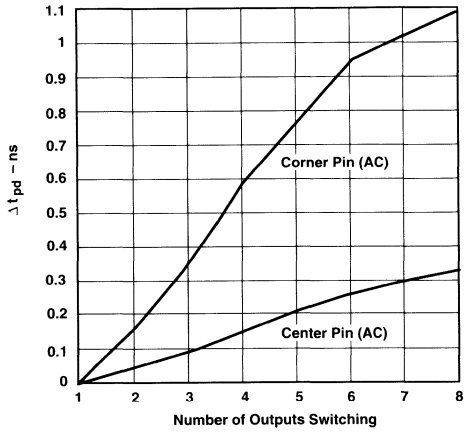


**Figure 19. Increase of the Delay Time When Several Outputs Are Switched Simultaneously**

With bus drivers and also VLSI circuits that have more than eight outputs that switch simultaneously, an appropriate number of additional supply-voltage pins are provided. A good example is given by the Widebus™ circuits from TI, which are bus drivers with 16, 18, or 20 outputs. To keep the loss of speed (because of so many outputs) within limits, about 25% of all pins of these devices are reserved for the provision of supply voltage. Figure 20 shows the increase of the delay time of a 74AC16240 as a function of the number of outputs that are switched simultaneously.

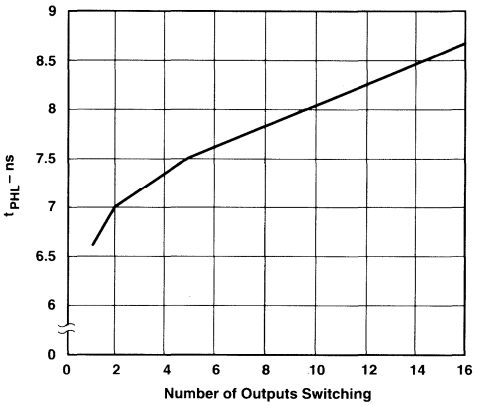


**Figure 20. Increase of the Propagation Delay Time With a Widebus™ Circuit (74AC16240)**

## 6.2 Propagation Delay Times With Negative Undershooting at the Outputs

With bipolar circuits, negative voltages caused by undershooting can influence the function of the device. Figure 21 shows this effect. This circuit represents the output stage of a bus driver, which should be in an inactive and high-impedance state. Active bus driver U1 switches the line between the two devices from a high to a low level. As a result of an inadequate termination of the line, there is a negative undershoot on the line, which causes a current ($I_X$) to flow in the internal circuit of the output stage. This current flows via the collector-base diode of transistor Q5 and Schottky diode D1, in parallel with it and via transistor Q1 to the base node of transistor Q2. Now this node is clamped to a low level. If this output stage should again be switched to the active state (output enable switches from low to high), the output does not follow until the capacitance of the bus line is charged through resistor R to the extent that the collector base diode of transistor Q5 is turned off again, which takes, typically, 5 ns to 10 ns. Apparently, the delay time to again switch on the output stage is increased by approximately this amount.

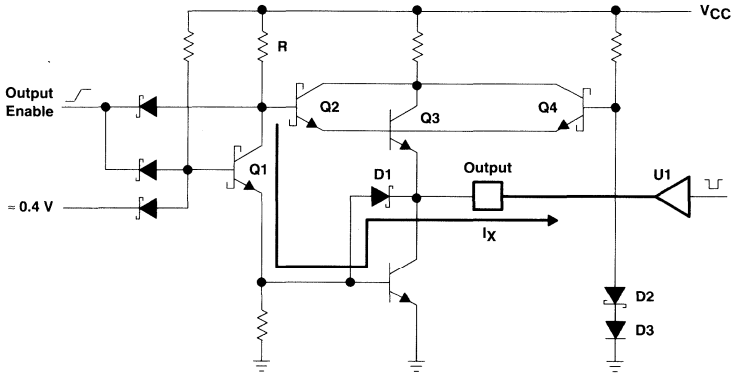


**Figure 21. Currents in the Output Stage of a Bus Driver With Negative Undershoot**

To prevent this delay, a clamping circuit (D2, D3, and Q4 in Figure 21) is integrated into modern bus drivers. This ensures that, should the output voltage go below –0.3 V, transistor Q3 switches on the output stage and the current $I_X$ is diverted to the positive supply-voltage rail $V_{CC}$. With ABT devices, clamping is unnecessary and a different circuit that can be more effective is used.

### 6.3 Propagation Delay Times With Large Capacitive Loads

In digital logic device data sheets, propagation delay times are specified with a capacitive load of 50 pF (15 pF on older logic families). This value represents the capacitive load of the test circuit on the output of the device being tested. This value is also the capacitive load when the output drives five inputs of other circuits and this assumes that the length of the connecting lines is only a few centimeters, as is typically the case on printed circuit boards (PCBs). With such short lines, the first assumption is that the line itself behaves like a capacitor, which additionally loads the output and influences the propagation delay time accordingly. However, with long lines, this assumption leads to errors, because the signal delay is actually determined by the propagation speed of the electrical wavefront along the line. In fact, the propagation delay time of the device is determined by the loading of the output, that is, by the characteristic impedance of the line to which it is connected, not by its length or capacitance. When driving a line terminated at its end with a resistance of 100 Ω and lengths of 0 (resistor connected directly to the output), 1 m, and 11 m (see Figure 22), an SN74LS00 device has the output waveforms shown in Figure 23. The three resulting output signals are shown staggered, and are practically identical, i.e., the propagation delay time of the device is not influenced. The length of the line and the resulting signal propagation time (5 ns/m) influence the delay time of the system. The propagation time of the wave along an 11-m transmission line is 55 ns. Add the propagation delay time of the SN74LS00 of about 10 ns for a total delay of 65 ns.

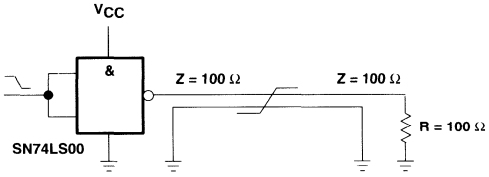


**Figure 22. Measurement Setup**

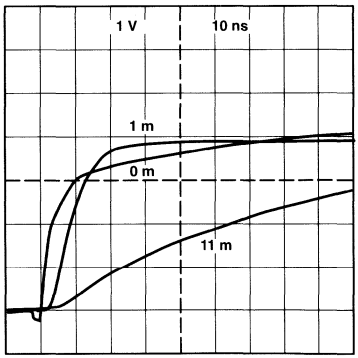


**Figure 23. Waveforms for Various Line Lengths**

If the capacitive load connected to the output of a device is represented as a single capacitor, the resulting propagation delay time can be calculated. A purely capacitive load can be assumed if the output of the device controls a MOS power transistor with a relatively large input capacitance. To a first approximation, this assumption is correct if an output drives adjacent inputs over a line length of only a few centimeters. The propagation delay times given in data sheets consider the following:

- Propagation delay time through the internal circuitry of the device
- Delay resulting from the switching time of the output stage
- Time needed to charge and discharge the capacitance of the load (typically 50 pF)

The first two considerations are independent of the load that is connected. The last consideration must account for the actual load, of which a load capacitance of C1 = 50 pF (15 pF) is already given in data sheets. The time taken to charge the additional capacitance is determined by the current that the device is able to deliver. For the high level, this value can be deduced indirectly from the data sheet. Figure 24 shows the relevant part of the circuit of a bipolar output stage and the resulting output characteristics.

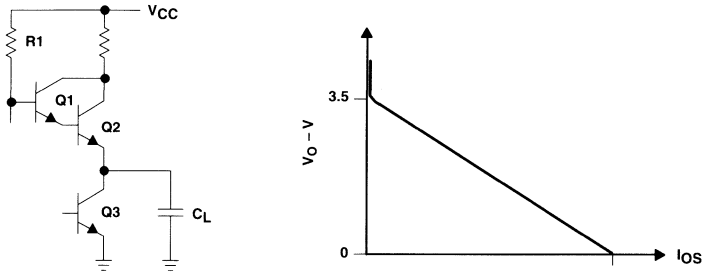


**Figure 24. Bipolar Output Stage With Output Characteristics at a High Level**

The short-circuit current of the output, when at a high level, is determined by the resistance (R1) and the saturation voltage of Darlington transistors Q1 and Q2 with collector-path resistance. Using the following equation, the internal resistance ($R_O$) of a circuit can be determined from the open-circuit output voltage (typically 3.5 V) and from the short-circuit current ($I_{OS}$) given in the data sheet:

$$R_O = \frac{3.5\ V}{I_{OS}} \quad (4)$$

With circuits that use MOS transistors in their output stages (SN74HC and 74AC/SN74AC), the output current is determined by the size of the transistors and the potential difference between gate and source. Since there is no linear relationship between this voltage and the output current, only an approximate indication of the output resistance can be made.

Table 2 shows $I_{OS}$ and $R_O$ for the most important device types.

**Table 2. Short-Circuit Current and Internal Resistance of Logic Families**

| TYPE | SHORT-CIRCUIT CURRENT $I_{OS}$ (mA) | INTERNAL RESISTANCE $R_O$ (Ω) |
|---|---|---|
| SN7400 | 35 | 50 |
| SN7440 | 45 | 75 |
| SN74LS00 | 35 | 100 |
| SN74LS40 | 65 | 53 |
| SN74LS240 | 70 | 50 |
| SN74S00 | 65 | 53 |
| SN74S40 | 140 | 25 |
| SN74S240 | 60 | 58 |
| SN74ALS00 | 50 | 70 |
| SN74ALS40 | 60 | 58 |
| SN74ALS240 | 100 | 35 |
| SN74ALS1000 | 120 | 29 |
| SN74AS00 | 100 | 35 |
| SN74AS240 | 140 | 24 |
| SN74AS1000 | 160 | 21 |
| SN74F00 | 85 | 41 |
| SN74F40 | 140 | 25 |
| SN74F240 | 140 | 25 |
| SN74BCT240 | 140 | 25 |
| SN74BCT25240 | 700 | 5 |
| SN74ABT240 | 120 | 29 |
| SN74HCT00 | 60 | 40–120 |
| SN74HCT240 | 80 | 30–100 |
| 74ACT11000 | 220 | 4–25 |
| 74ACT11240 | 220 | 4–25 |
| SN74LV00 | 35 | 35–100 |
| SN74LV240 | 55 | 25–80 |
| SN74LVC00 | 85 | 16–40 |
| SN74LVC240 | 85 | 16–40 |
| SN74LVT240 | 400 | 8 |

The typical output voltage of a bipolar device at a low level is about $V_{OL} = 0.3$ V. The increase of the delay time resulting from the capacitive load ($C_L$) is determined by the time until the external load capacitance has been charged by an external voltage source from $V_{OL}$ to the threshold voltage of the circuit, typically $V_S = 1.5$ V. The external voltage source is described by an internal voltage ($V_{OH}$) and an internal resistance ($R_O$). In this way, the delay time ($t_d$) resulting from the load capacitance can be calculated from the following equation:

$$t_d = \ln\frac{V_{OH} - V_{OL}}{V_{OH} - V_S} \times R_O \times C_L = \ln\frac{5.5\ \text{V} - 0.3\ \text{V}}{3.5\ \text{V} - 1.5\ \text{V}} \times R_O \times C_L = 0.5 \times R_O \times C_L \quad (5)$$

Figure 25 shows the waveform of the positive edge at the output of a gate (SN74LS00) with various values of capacitive loads ($C_L$ = 10 pF, 56 pF, and 616 pF). As expected, the rise time at the output and the resulting increase of the propagation delay time are determined by the time constant $R_O \times C_L$.

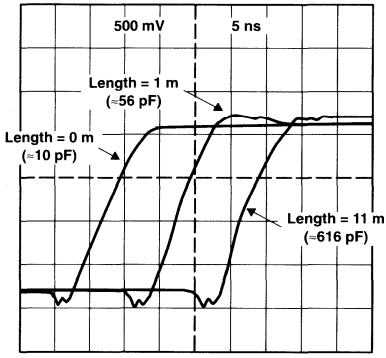


**Figure 25. Waveform at SN74LS00 Output ($C_L$ = 10 pF, 56 pF, and 616 pF)**

The values for the low level of a bipolar device cannot be taken directly from data sheets. Transistor Q3 in Figure 24 is responsible for the output current $I_{OL}$. As with all semiconductor components, this parameter is nonlinear, and is influenced by the distribution of components in the circuit on such parameters as current gain, conductance, and resistance values. For this reason, only a rough calculation of the actual output current at low level is possible. As a first approximation, the internal resistance of the circuit at low level is lower than at high level. It follows that, in the worst case, the increase of the delay time of the negative edge is always smaller than that of the positive edge (see equation 5). The precise value must be determined in individual cases by measurement.

### 6.4 Input and Output Capacitances of Digital Devices

All digital devices capacitively load the outputs of the circuits driving them. The input and output capacitances are given in Table 3. These are typical average values for the logic families shown. Different circuit configurations are used within a family, depending on the function and application. Therefore, wide variations from the values given in data sheets can occur with individual devices. In specific cases for new families, the values given in data sheets should be taken as a basis. If this data is not available, for example with older families, the user must make appropriate measurements if more precise values are needed.

The capacitances given in Table 3 are measured at the following voltages:

- Bipolar devices: V = 2.5 V
- CMOS devices: V = 0 V and V = 2.5 V

**Table 3. Capacitances of Digital Devices**

| FAMILY | INPUT CAPACITANCE (pF) | OUTPUT CAPACITANCE (pF) | |
|---|---|---|---|
| | | OPEN-COLLECTOR OUTPUT† | BUS DRIVER |
| SN74 | 3 | 5 | – |
| SN74LS | 3.5 | 3.5 | 5 |
| SN74S | 3.5 | 3.5 | 9 |
| SN74ALS | 2 | 4 | 5 |
| SN74AS | 4 | – | 10 |
| SN74F | 5 | 5 | 9 |
| SN74HC | 3 | 3 | 9 |
| 74AC/SN74AC | 4 | – | 10 |
| SN74BCT | 6 | – | 12 |
| SN74ABT | 4 | – | 8 |
| SN74LV | 3 | – | 8 |
| SN74LVC | 4 | – | 8 |
| SN74LVT | 4 | – | 8 |

† Open-collector output of gates and other devices with low drive capability (e.g., SN74xx03). Open-collector outputs of bus drivers have the same output capacitance as totem-pole (3-state) outputs.

## 7 Bus Contention

If several bus drivers with 3-state outputs are connected to a single bus, it often cannot be ensured that during the time when switching from one bus driver to another, both are not simultaneously active for a short time. For this short time, a short circuit of the outputs exists, resulting in an overload of the circuit. This situation is known as *bus contention*.

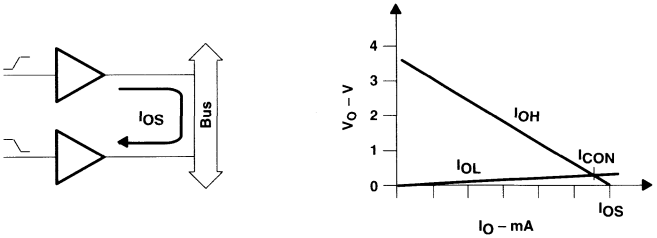


**Figure 26. Determining the Short-Circuit Current With Bus Contention**

The currents that result from bus contention can be calculated by means of the output characteristics of the devices (see Table 2). As shown in Figure 26, the short-circuit current ($I_{OS}$) is limited by the high-output current of the devices involved in bus contention. With bus drivers having an output current of $I_{OL}$ = 64 mA (SN74AS, SN74F, SN74BCT, SN74ABT, or SN74LVT), a current $I_{OS}$ = 120 mA flows in such a case. The power dissipation ($P_{conl}$) of the output supplying the low level, as shown below, can be ignored.

$$P_{conl} = V_{OL} \times I_{OS} = 0.5\ V \times 120\ mA = 60\ mW \quad (6)$$

Even if all eight outputs of a bus driver are involved in bus contention, the total power dissipation is less than 500 mW. However, the situation is different at the outputs supplying the high level. In this case, the short-circuit power dissipation ($P_{conh}$) of each output is as follows:

$$P_{conh} = (V_{CC} - V_{OL}) \times I_{OS} = 4.5\ V \times 120\ mA = 0.54\ W \quad (7)$$

If all eight outputs of a bus driver are involved in this bus contention, the total power dissipation is about 5 W. With Widebus circuits, it is 10 W and more.

To analyze the situation inside a device under these extreme conditions, one has to know that the heat caused by this power dissipation is not immediately spread over the total chip. Rather, one has to consider a certain propagation speed of the heat, which is about 1 µm/µs. This means that during bus contention with a duration of only a few nanoseconds, the heat is not distributed over all the chip. In the first moment, the affected component inside the device (the transistor or resistor) heats up. The resulting increase in temperature can be calculated by knowing the volume of the component in question and the thermal capacitance of silicon. By using the output stage of an ABT device (see Figure 27), this is shown in detail. Also, all voltages are shown in this circuit diagram that apply when the output, which should provide a high level, is forced to 0.5 V externally.

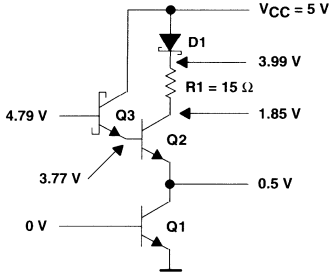


**Figure 27. ABT Output-Stage Circuit Diagram**

Table 4 shows the conditions in this output stage during bus contention. When calculating the volume of the single components, only that volume was considered that is related to the function of the component. For example, a transistor's total area was taken into account, but only the junction width, where the heat is dissipated, was considered as the component's height.

**Table 4. Output-Stage Conditions During Bus Contention**

| | VOLTAGE V (V) | CURRENT I (mA) | POWER DISSIPATION P (W) | VOLUME V ($\mu m^3$) | POWER DISSIPATION/ VOLUME ($W/\mu m^3$) |
|---|---|---|---|---|---|
| D1 | 1.01 | 142 | 0.156 | 3200 | $46 \times 10^{-6}$ |
| R1 | 2.14 | 142 | 0.304 | 3840 | $79 \times 10^{-6}$ |
| Q2 | 1.35 | 142 | 0.192 | 495 | $38 \times 10^{-3}$ |

According to this analysis, the highest power dissipation per volume unit is found in transistor Q2. This is because the junction width of only 0.5 µm was considered as the height of this component. Using equation 8, calculate the temperature increase ($\Delta\vartheta$):

$$\Delta\vartheta = \frac{P \times t}{V \times c_P} \tag{8}$$

Where:

$c_P$ = heat capacitance of silicon = $1.631 \times 10^{-3}$ Ws/Kmm$^3$
P = power dissipation
t = time
V = volume

Considering a propagation speed of the heat of 1 µm/µs and a junction width of 0.5 µm, one can assume that during the first 500 ns of bus contention the heat is not distributed over the chip, but stays in the transistor junction. Under this condition, $\Delta\vartheta$ is calculated as follows:

$$\Delta\vartheta = \frac{0.192\ W \times 500\ ns}{495\ \mu m^3 \times 1.631 \times 10^{-3} \frac{W \times s}{K \times mm^3}} = 119\ K \tag{9}$$

Short bus contention, with a duration of a few, or of a few tens of nanoseconds, causes a temperature increase of the component in question of about 10°C. Therefore, a degradation of the reliability of the component is unlikely. Furthermore, in well-designed systems, the period of bus contention is high compared to the duration of a single instance of bus contention (period:duration > 10:1). Conservatively, the mean chip temperature should be calculated to ensure that this temperature does not increase beyond 150°C. Beyond this temperature, the thermal expansion coefficient of the plastic material of the package becomes different from the expansion coefficient of silicon. This fact is likely to lead to a mechanical stress at high temperatures, which can result in failure of the bond wire.

The total power dissipation ($P_T$) of a bus driver is calculated by the following equation:

$$P_T = P_O + (P_S \times t_S + P_C \times 2\tau + P_{con} \times t_{con}) \times f \times n \tag{10}$$

Where:

f = frequency
n = number of outputs at which bus contention occurs
$P_{con}$ = power dissipation during bus contention
$P_C$ = power dissipation when discharging the bus capacitance
$P_O$ = quiescent power dissipation
$P_S$ = power dissipation resulting from current spikes when output switches
$t_{con}$ = duration of bus contention
$t_S$ = duration of current spike
$\tau$ = signal propagation time on the bus

The power dissipation of a bus driver is calculated in a practical example in accordance with the following assumptions:

- Circuit: SN74F245
- $P_O$ = 0.45 W (from data sheet)
- $P_S$ = 5 V × 30 mA = 0.15 mW with $t_s$ = 5 ns (measured)

To calculate the power dissipation ($P_C$) that occurs when charging the capacitance of the bus line, the voltage waveform at the output with the given load (the line impedance) must be known. The easiest way to determine this is to use the Bergeron diagram. With a line impedance of 30 Ω a stable state is reached after double the time of the signal propagation with a positive edge. That is, for this time, a current is supplied into the line from the driver circuit. The amplitude of the preceding waveform and the output voltage of the circuit is about $V_O = 2$ V. The power dissipation during this time and under these load conditions is calculated as follows:

$$P_C = (V_{CC} - V_O) \times \frac{V_O}{Z_O} = (5\ V - 2\ V) \times \frac{2\ V}{30\ \Omega} = 0.2\ W \quad (11)$$

The signal propagation time on a backplane in a 19-inch rack (wire length about 40 cm) is $\tau = 10$ ns.

Further, assuming a bus cycle time of 100 ns (f = 10 MHz), a bus-contention duration of 10 ns, and that all eight outputs of the device are involved, the resulting total power dissipation is calculated as follows:

$$\begin{aligned} P_T &= 0.45\ W + (0.15\ W \times 5\ ns + 0.2\ W \times 2 \times 10\ ns + 0.53\ W \times 10\ ns) \times 10\ MHz \times 8 \\ &= 0.45\ W + (0.75\ nW/s + 4\ nW/s + 5.3\ nW/s) \times 10\ MHz \times 8 \\ &= 1.29\ W \end{aligned} \quad (12)$$

This power dissipation results in a rise of the temperature of the chip, which, in turn, influences the reliability of the device. The chip temperature can be calculated as follows:

$$T_J = T_A + P_T \times R_{\Theta JA} \quad (13)$$

Where:

$R_{\Theta JA}$ = thermal resistance of package
$T_A$ = ambient temperature
$T_J$ = chip temperature

Table 5 shows the typical thermal resistance of the packages, which are mostly used for digital devices. These must be considered as typical values, because a number of factors determine the actual value, including chip size, lead-frame material, composition of the plastic, ambient air flow, and thermal properties of the circuit board. The values given apply if the device is soldered onto a PCB.

**Table 5. Thermal Resistance of Plastic Packages in Still Air**

| NO. OF PINS | THERMAL RESISTANCE (°C/W) | |
|---|---|---|
| | DL PACKAGE | SO PACKAGE |
| 14 | 86 | 117 |
| 16 | 80 | 110 |
| 20 | 78 | 95 |
| 24 | 73 | 85 |

According to Table 5, the thermal resistance of a 20-pin DL package is $R_{\Theta JA} = 78$°C/W. This means that, in equation 8, the chip temperature would be about 100°C above the ambient temperature. The chip temperature must not be allowed to exceed 150°C, because the reliability would be reduced significantly. Therefore, the maximum permissible ambient temperature is, in this case, 150°C – 100°C = 50°C.

In cases in which bus contention can occur, which is in most bus applications, power dissipation is of particular importance. There is usually nothing that can be done about dynamic conditions (the frequency of operation) without adversely affecting the performance of the system. Also, the overlap of operating states cannot always be prevented if worst-case conditions are taken into account. However, bus contention of a duration of a few, or of a few tens of nanoseconds should not be a problem. The choice of the most suitable components allows control of the quiescent power dissipation. With fast bipolar logic families (SN74S, SN74AS, and SN74F), the permissible total power dissipation might be exceeded because of their high quiescent power dissipation. Better, in this respect, are the SN74LS and SN74ALS series because, with their lower quiescent-current requirements, bus contention does not result in overdissipation in most cases. Even better are devices from the BiCMOS series and all CMOS devices, although in CMOS parts, a part of the advantage of their low quiescent current is lost by their higher dynamic power dissipation.

One critical application area is bus contention during the power-on phase of a system. This bus contention occurs because, during the power-on phase (system reset), the supervising circuit does not provide defined control signals even though the rest of the system may already be functional. Therefore, there is a high probability that various bus drivers might be accidentally activated at the same time. This, again, results in bus contention that can last several 100 ms (duration of the power-on phase or reset time). Because the thermal time constant of a device is about 1 ms to 5 ms, after this time expect the final temperature in the device to be determined by momentary power dissipation. If a total power dissipation of 5 W in an 8-bit device during this bus contention is assumed, a theoretical 500°C overtemperature of the chip must be considered. With Widebus circuits, the theoretical overtemperature is 1000°C. Mostly, these devices are immediately destroyed during these kinds of bus contention. Even if no defect is detected after such bus contention, a dramatic degradation of the device is likely, which leads to a final destruction of the component some time later.

An adequate design of the control logic prevents bus contention during the power-on phase of a system. Preventing bus contention is not easy because no defined supply voltage can be expected during the power-on phase. Therefore, no defined operation of the logic circuits can be expected. The supply-voltage range below 3 V usually is not critical. Many advanced bus drivers contain a supply-voltage monitor that disables the outputs (3-state) as long as the supply voltage is lower than about 3 V. Furthermore, below this voltage, an overload of the devices is unlikely, because under this condition, the drive capability is very limited. Above a supply voltage of 3 V, additional measures are necessary. One method is to connect a pullup resistor between the enable inputs of the bus-interface circuits and the positive supply rail. This may ensure a high level as long as the preceding control logic does not provide a defined logic level, but is not helpful if the control logic delivers a wrong logic level. A reliable solution is to disable all bus-interface circuits in question during the critical time with additional control logic (see Figure 28). In this circuit, a supply-voltage monitor (TLC7705) provides a signal that disables all bus drivers during the critical time period and may reset the main processor, which then resets the control logic of the system. For this kind of application, bus-interface circuits that provide two enable inputs, like the SN74ABT541, are advantageous. One control input controls the normal operation via the system-control logic. The other input is connected to the monitor device to disable the bus logic when an undefined system condition (e.g., during power on) is expected. If no second enable input is available, such as in an SN74ABT245, another gate is required to perform the additional disable function.

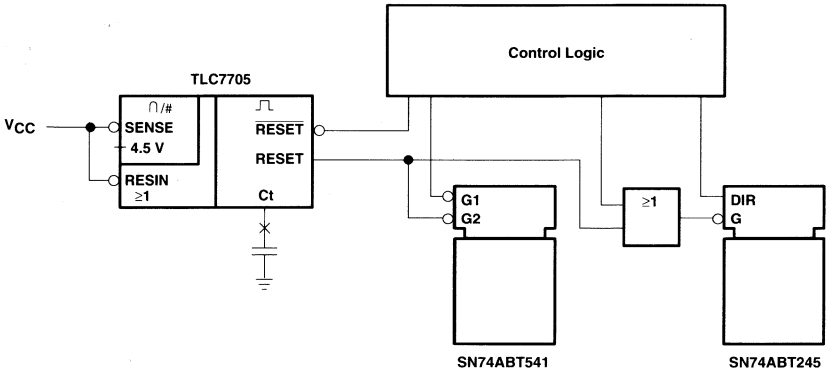


**Figure 28. Bus Supervision During Power On**

**CAUTION:**

Since considerably higher currents flow on signal lines during bus contention than with normal operation, the noise margin in the system is reduced accordingly. This can result in faulty operation and care should be taken to avoid bus contention.

## 8 Backdriving

The testing of highly complex electronic systems must ensure that the system or subsystem operates faultlessly. For this purpose, it is advantageous to install at the system level diagnostic programs that are able to recognize and localize faults. Certain limitations are unavoidable with self-testing because a defective system may no longer be able to seek and localize faults. This method usually breaks down completely when individual component groups are being tested because fault diagnosis on their own is generally too limited. In such cases, additional test equipment that stimulates the component group with special test signals, test samples, or patterns, and analyzes the results is necessary.

If all relevant circuit segments in the component group can be addressed via a defined interface, e.g., built-in testability (BIT), testing can be performed without additional test circuits and adapters. Test bus IEEE Std 1149.1 (JTAG), with an appropriate device interface, allows testing of all circuits, the connections between them, and the complete subsystem.

If this option is not available, appropriate signals can be injected into the circuit from outside to achieve the required circuit stimulation. For this, the inputs to the circuits to be tested must be supplied with the necessary voltages (e.g., logic low or high) via nail-bed adapters and the reaction at the outputs of these circuits is monitored. In this way, the functions of complex systems can be tested step by step and the most common faults recognized, such as:

- Solder bridges and broken metallization
- Incorrect, faulty, damaged, or missing devices
- Functional disturbances and signal-processing faults

Because only a few single devices are accessed at a time, only the special, appropriate functions (e.g., the truth table of a gate) need to be known, not the function of the complete device group. In this way, standard test program libraries can be used to put together the complete test program. With this method, large systems also can be tested step by step without using excessively complex test procedures.

The stimulation of the circuit to be tested might present a problem. For example, the inputs of gate G3 (see Figure 29) must be switched to a particular potential. These same inputs are already controlled by other devices (G1 and G2), which supply their own signals to the gates to be tested. The test equipment must be able to force another voltage on to the same node as is supplied by the existing circuit. The expression commonly used here is *backdriving* or *node forcing*. The output of a device is forced from outside into a state not corresponding to its normal control-logic state.

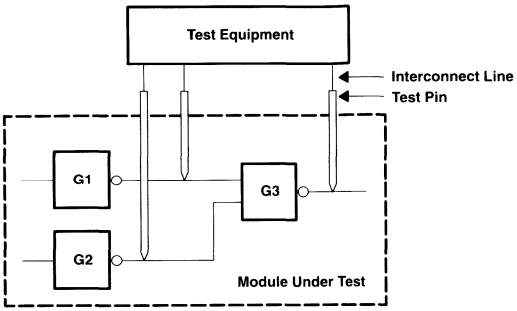


**Figure 29. Feeding Test Signals Into a Node Test Point**

The test equipment must have substantial drive capability to force the device into another logic state. Table 2 gives the short-circuit current at high level of the most important logic families. The situation in which the test equipment must force an output to low level is not the most demanding requirement. Currents of up to several-hundred milliamperes must be provided to force from outside an output that is supplying a low level into a high-level state.

Serious interference arises when the high currents are switched on or off and line reflections occur on the lines connecting the test equipment and the circuit being tested. All these effects can result in a real or apparent malfunction of the circuit being tested. This test method is of limited use when the precise timing of fast circuits must be assessed.

When injecting the test-signal current into the outputs, which then must be forced into an inverted state, the devices usually are driven far outside their maximum permissible ratings. This can damage or destroy the devices. At the very least, their reliability and, therefore, their operating life, is adversely affected. In recent years, the drive capability (maximum output currents) of devices has been steadily increased in the interest of improved technical performance. Modern bus-driver currents of 500 mA and more are needed to force the outputs of devices to particular logic levels (see Figure 30). The high current densities in the internal connections of devices can cause a drift of metallic ions, or so-called electromigration. This effect begins at current densities of $3 \times 10^5$ to $10^6$ A/cm$^2$. Metallic ions are released from the grain boundaries and then drift in the inverse direction of current flow (in the direction of the electron flow). If the excessive current density lasts long enough, the interconnections are eroded.

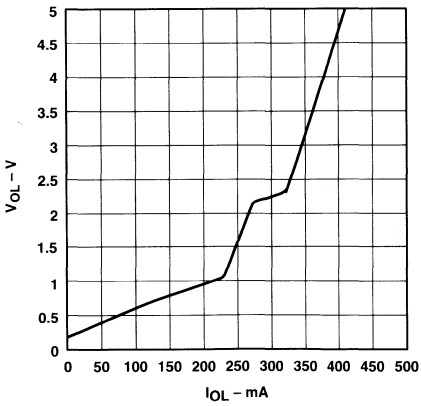


**Figure 30. Low-Logic-Level Output Characteristics of SN74AS645**

When backdriving, the most important effect is the extreme rise in temperature that occurs in the chip during the test. The heat that results must be conducted away via the package. The equivalent circuit of Figure 31 shows the thermal relationships in the package.

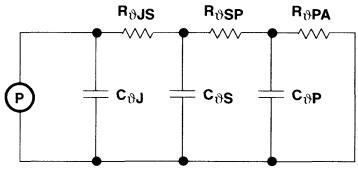


**Figure 31. Thermal Resistances in a Device**

The thermal source (P) first fills up the thermal capacitance of the semiconductor junction. The heat spreads, via $R_{\vartheta JS}$, in the complete substrate (chip) of the device. From there, the heat flows, via the resistance ($R_{\vartheta SP}$), into the package and then, via the resistance ($R_{\vartheta PA}$), to the ambient environment. Only the sum of the thermal resistances $R_{\vartheta JU} = R_{\vartheta JS} + R_{\vartheta SP} + R_{\vartheta PA}$ (thermal-resistance junction ambient) is given in data books (see Table 5). This resistance is not helpful for the problem under consideration but it can be used to calculate the temperature in a stable state. Rapid temperature increases, such as result from backdriving, cannot be calculated from the sum of thermal resistances. The thermal capacitance and thermal conductivity of the chip can be calculated, but it is better to determine the thermal behavior through measurements (see Figure 32).

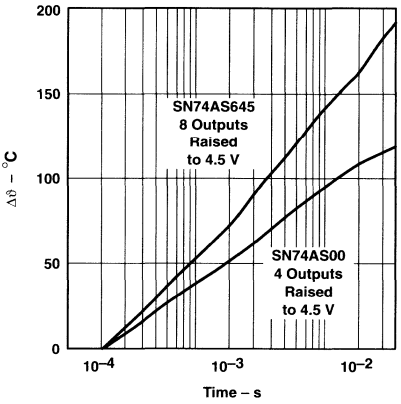


**Figure 32. Device Thermal Behavior**

Figure 32 shows that, with an SN74AS645, a temperature rise in the chip of 100°C must be expected after 2 ms. After 10 ms, temperatures are attained that are not permissible in plastic packages. CMOS and BiCMOS circuits have a very low power dissipation and do not behave better in this particular case. With these modern components, expect at least the same driving capability. The short-circuit current at the output of an ACL logic device is >250 mA. It is ultimately these currents that are responsible for the high power dissipation during backdriving.

The following rules always should be observed when using the test methods discussed:

- Backdriving should be used only when the state required at the node point in question can be reached in no other way.
- The maximum permissible power dissipation of a device should not, under any circumstances, be exceeded.
- Outputs that are at a low-level state, as a result of their logic functions, can be raised to a level of $V_O = 3$ V for a short period by backdriving. The energy, which as a result of this backdriving is injected into the device ($V_O \times I_{OL} \times t_{pd}$), must not exceed 25 mW/s. The current that results in an output should not exceed a value of $I_{OL} = 300$ mA. The pulse duration must not exceed $t_d = 100$ ms. To keep the thermal stress within acceptable limits, the duty cycle of the pulses (duration of the pulse ÷ duration of the period) should be less than 1:10.
- Outputs that are in a high-level state as a result of their logic functions can be lowered to a level of 0 V for a short time by means of backdriving. One output of a device can be short circuited to ground, in such a case, for maximum $t_d = 100$ ms. The product of the output current, the supply voltage, and the pulse duration ($I_{OH} \times V_{CC} \times t_{pd}$) must not exceed 25 mW/s. If n outputs are simultaneously short circuited to ground, limit the total energy injected into the device under test ($I_{OH} \times V_{CC} \times t_{pd}$) to 25 mW/s. To keep the thermal stress within reasonable limits, the duty cycle of the short circuit (short-circuit duration ÷ repetition time) should be less than 1:10.
- All voltages, including peak voltages of overshoots/undershoots, must be within the absolute maximum ratings on data sheets.
- Simultaneous backdriving of several outputs in parallel (wired OR) with a common current source is not permissible. Since current sharing cannot be predicted, there is danger of overloading the circuit.
- The chip temperature of the circuit under test must not exceed 125°C.
- Open-circuit (unterminated) lines should be avoided to prevent faults caused by reflection.

Semiconductor device manufacturers consider testing with backdriving as involving a measure of risk. The danger of overloading devices cannot be excluded since they are operated in regions that can lie far outside those for which they were designed. For this reason, no statement about the reliability of devices that are subjected to this test procedure can be made. TI does not use such test methods. Such test methods are not permissible in many (e.g., military) areas of application.

## 9 Summary

This report provides the designer of digital systems information that is not found in data books, but which is of interest and necessary in many applications. The differences between individual circuit families have been discussed. The circuit design techniques used with various devices, combined with the different technologies used to manufacture them, often make it difficult to give specific design rules; in many cases it is possible to give only very general guidance. In practice, few parameters are actually measured, particularly with older devices. In all such cases, this report provides guidelines that enable the designer to predict the behavior of circuits in a system.

## Acknowledgment

The author of this document is Eilhard Haseloff.

# *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*

SCZA005A
June 1997

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## Contents

## Thermal Considerations for Standard Linear and Logic (SLL) Packages and Devices

Users of Texas Instruments (TI™) SLL products must consider device power dissipation, package power capability, and maximum ambient temperatures when designing with these products. The product users also need to be aware of the long-term reliability impact of maximum device-junction temperatures.

This application report is intended to help users understand and evaluate these factors. Three concepts — package thermal performance, device power dissipation, and reliability — are discussed in separate sections.

The first section, *Package Thermal Performance*, includes data about the recently developed EIA/JEDEC Standard JESD 51 for package thermal-impedance measurement. It discusses most SLL package types and lists $\theta_{JA}$ (thermal impedance) values for those packages.

The second section, *Power Calculation*, discusses the power consumption by CMOS and BiCMOS/bipolar semiconductors. Standard formulas are given that allow the user to calculate the maximum power dissipated by a device in a typical application using data-book specifications, operating frequency, and voltage. The only characteristic not readily known is the output loading of the devices under consideration.

The third section, *Benefits of Minimizing Power Consumption*, discusses ways to reduce power consumption and the benefits thereof.

The final section, *Reliability Implications*, discusses the effects of chip temperature on reliability and electromigration. Information presented in this section allows the user to make an informed judgment as to the maximum chip temperature versus device wearout acceptable in the particular application.

The recommended analysis procedure is to assume a maximum chip temperature (see *Reliability Implications*) then, using $\theta_{JA}$ values for the chosen package (see *Package Thermal Performance*) and the known environmental requirements, calculate the maximum permissible power for that package. The formula presented in the *Power Calculation* section can then be used to ensure the operating conditions do not exceed the power capability of the chosen package type. Of course, the user can choose to calculate the maximum power from the application, then select a package that can meet the power dissipation requirement.

## Package Thermal Performance

The most common measure of package thermal performance is thermal impedance ($\theta_{JA}$) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for $\theta_{JA}$ is:

$$\theta_{JA} = \frac{T_j - T_a}{P} \quad (1)$$

Where:

$T_j$ = chip junction temperature
$T_a$ = ambient temperature
P = device power dissipation

$\theta_{JA}$ values are also the most subject to interpretation. Factors that can greatly influence the measurement and calculation of $\theta_{JA}$ are:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

JEDEC established the JC 15.1 committee, comprising industry representatives, to develop industry-standard specifications for thermal testing. The specifications include development of electrical test procedures, careful descriptions of appropriate test environments, guidelines for the design of thermal test chips, guidelines for thermal modeling, and specifications for component mounting. The specifications for component mounting are divided into a series for different package types. The specifications include test-board descriptions for low effective thermal-conductivity test boards with a single metal layer and high effective thermal-conductivity test boards with embedded solid copper planes simulating system power and ground planes.

In August 1996, the Electronics Industries Association released JESD 51-3 titled *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. The standard describes guidelines with parameters for thermal-test-board design for low effective thermal conductivity (one signal layer in the trace fanout area) as differentiated from a multilayer printed-circuit board (PCB), which might include power and ground planes. The specified parameters include the area of the test board, the amount of copper traces on the test board, and the resulting trace fanout area, each important to the heat-sinking characteristics of the PCB. Prior to release of the standard, thermal-impedance data for similar packages varied widely within the industry due to the use of different test-board designs. As the industry adopts this standard methodology, thermal-impedance variations from test-board design should be minimized.

Key features of the standard test-board design are:

- Board thickness: 0.062 in.
- Board dimensions: 4.0 × 4.5 in. for packages > than 27 mm in length, 3.0 × 4.5 in. for packages ≤ 27 mm in length
- Trace thickness: 0.0028 in.
- Trace length: 25.0 mm (0.984 in.)

The SLL product group uses test boards designed to JESD 51-3 for thermal-impedance measurements. The parameters outlined in the standard also are used to set up thermal models. The thermal-model program used by SLL is ThermCAL, a finite-difference thermal-modeling tool.

Eleven SLL packages were tested using a JEDEC test-board design and compared to ThermCAL model results to validate the correlation between model results and data (see Table 1). This comparison shows that the models are accurate to within 10% of measured data. In many cases the model data varies from measured data by less than 5%.

**Table 1. Package Comparison**

| PACKAGE TYPE (PINS, DESIGNATION) | DIE SIZE (mils) | $\theta_{JA}$ MEASURED (°C/W) | $\theta_{JA}$ MODELED (°C/W) | CHANGE (%) |
|---|---|---|---|---|
| 56 DL | 120 × 120 | 73.5 | 78.3 | 6.5 |
| 20 DW | 62 × 62 | 96.6 | 90.9 | –5.9 |
| 160 PCM | 240 × 240 | 34.9 | 34.9 | 0 |
| 52 PAH† | 120 × 120 | 87.2 | 92.2 | 5.7 |
| 52 PAH‡ | 120 × 120 | 72.7 | 75.2 | 3.4 |
| 100 PZ | 360 × 360 | 45 | 42.8 | –4.9 |
| 208 PDV | 240 × 240 | 50.1 | 52.8 | 5.4 |
| 48 DGG | 120 × 120 | 89.1 | 93.5 | 4.9 |
| 14 DGV | 62 × 62 | 181.5 | 191.7 | 5.6 |
| 48 DGV | 62 × 186 | 92.9 | 89.9 | –3.2 |
| 100 PCA | 240 × 240 | 33.3 | 34.9 | 4.8 |

† S-pad leadframe
‡ Conventional leadframe

After the accuracy of the model results was established, all other SLL packages could be modeled. $\theta_{JA}$ data based on JESD 51-3 is available for all SLL leaded surface-mount packages (see Table 2). The data is grouped by package type with values of $\theta_{JA}$ shown at different airflow levels. Leadframe pad size and die size are shown.

Junction-to-case thermal-impedance ($\theta_{JC}$) data is shown with the junction-to-ambient data. Measured $\theta_{JC}$ data was generated for the packages tested using the JEDEC PCB. Previously published values of $\theta_{JC}$ are used for packages not yet tested using the PCB designed to JESD 51-3.

## Table 2. SLL Package Thermal-Impedance Data

| PIN COUNT | TI PACKAGE | JEDEC SPECIFICATION | PAD SIZE (mils) | CHIP SIZE (mils) | $\theta_{JA}$ (°C/W) AT AIRFLOW (LFM) | | | | MEASURED/ MODELED | $\theta_{JC}$ (°C/W) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0 | 150 | 250 | 500 | | |
| **SOIC** | | | | | | | | | | |
| 14 | D | MS-012 | 70 × 70 | 32 × 37 | 126.6 | 104 | 96.4 | 87.4 | Modeled | 46 |
| 16 | D | MS-012 | 90 × 90 | 44 × 65 | 112.6 | 91.2 | 83.9 | 74.8 | Modeled | 42 |
| 20 | DW | MS-013 | 90 × 110 | 62 × 62 | 96.6 | 82.2 | 77.7 | 71.5 | Measured | 38.3 |
| 24 | DW | MS-013 | 140 × 160 | 84 × 122 | 80.7 | 53.7 | 47.5 | 40.7 | Modeled | 25 |
| 28 | DW | MS-013 | 120 × 140 | 90 × 128 | 78.2 | 54.3 | 48.4 | 41.9 | Modeled | |
| **SSOP** | | | | | | | | | | |
| 14 | DB | MO-150 | 71 × 71 | 43 × 52 | 158 | 128.6 | 118.9 | 106.5 | Modeled | 47 |
| 16 | DB | MO-150 | 83 × 91 | 51 × 61 | 130.8 | 105.9 | 97.3 | 86.5 | Modeled | 47 |
| 20 | DB | MO-150 | 87 × 106 | 61 × 65 | 114.6 | 92 | 84 | 74.7 | Modeled | 45 |
| 24 | DB | MO-150 | 87 × 106 | 74 × 91 | 104.2 | 83.5 | 76.3 | 67.5 | Modeled | 42 |
| 28 | DL | MO-118 | 150 × 180 | 97 × 142 | 97 | 77.2 | 70.9 | 63.1 | Modeled | |
| 48 | DL | MO-118 | 120 × 180 | 73 × 128 | 93.5 | 69.9 | 63.8 | 57.1 | Modeled | 26 |
| 56 | DL | MO-118 | 150 × 220 | 120 × 120 | 73.5 | 62.3 | 59 | 54.6 | Measured | 27.3 |
| **QSOP** | | | | | | | | | | |
| 20 | DBQ | MS-137 | 96 × 140 | 61 × 75 | 118.1 | 95.3 | 86.9 | 76.7 | Modeled | 46 |
| 24 | DBQ | MS-137 | 96 × 140 | 61 × 75 | 113 | 92 | 84.1 | 74.6 | Modeled | 42 |
| **PLCC** | | | | | | | | | | |
| 28 | FN | MS-018 | 300 × 348 | 214 × 319 | 70.9 | 58.8 | 52.7 | 46 | Modeled | 26.7 |
| 44 | FN | MS-018 | 270 × 270 | 235 × 235 | 46.2 | 38.6 | 35.4 | 31.6 | Modeled | 22 |
| 68 | FN | MS-018 | 325 × 325 | 280 × 280 | 39.3 | 33 | 30.5 | 27.6 | Modeled | 14.5 |
| 84 | FN | MS-018 | 275 × 275 | 188 × 185 | 39.7 | 33.9 | 31.8 | 29.4 | Modeled | 11.9 |
| **QFP** | | | | | | | | | | |
| 52 | RC | MS-022 | 210 × 210 | 120 × 120 | 78.9 | 48.4 | 43.6 | 38.1 | Modeled | 20 |
| 80 | PH | | 265 × 265 | 232 × 240 | 76.1 | 67.9 | 61.4 | 53.6 | Modeled | 15.1 |
| 132 | PQ | MO-069 | 315 × 315 | 272 × 272 | 46.3 | 34.5 | 31.6 | 28.3 | Modeled | 9.8 |
| 144 | PCM | MS-022 | 433 × 433 | 338 × 338 | 38.8 | 27.3 | 25.1 | 22.4 | Modeled | 14.5 |
| 160 | PCM | MS-022 | 511 × 511 | 433 × 433 | 34.9 | 29.9 | 28.3 | 24.7 | Measured | 11.4 |
| 208 | PPM | MO-143 | 413 × 413 | 268 × 268 | 36.7 | 30.4 | 28.1 | 26.7 | Modeled | |
| **TQFP** | | | | | | | | | | |
| 52 | PAH | MO-136 | S-Pad | 120 × 120 | 87.2 | 76.1 | 71.5 | 67 | Measured | 28.3 |
| 52 | PAH | MO-136 | 3.5 × 3.5 mm | 120 × 120 | 72.7 | 62.6 | 59.2 | 53.8 | Measured | 24.0 |
| 64 | PM | MO-136 | 6.75 × 6.75 mm | 235 × 235 | 66.9 | 53.6 | 47.6 | 40.6 | Modeled | 10.4 |
| 64 | PAG | MO-136 | S-Pad | 240 × 240 | 58.2 | 48.8 | 45.2 | 40.3 | Measured | 22.6 |
| 80 | PN | MO-136 | S-Pad | 240 × 240 | 61.5 | 52.8 | 49.3 | 44.6 | Measured | 26.4 |
| 100 | PZ | MO-136 | S-Pad | 360 × 360 | 45 | 38.3 | 35.3 | 27.9 | Measured | 7.6 |
| 100 | PZ | MO-136 | S-Pad | 240 × 240 | 50.1 | 42.7 | 40.4 | 36.8 | Measured | 21.1 |
| 100 | PCA | MO-136 | 6.5 × 6.5 mm | 240 × 240 | 33.3 | 24.7 | 21.8 | 19.2 | Measured | 4.3 |
| 120 | PCB | MO-136 | 6.5 × 6.5 mm | 240 × 240 | 28.1 | 22.3 | 21 | 18 | Modeled | 3.3 |
| 144 | PGE | MO-136 | 342 × 350 | 378 × 378 | 48.3 | 39.1 | 35.5 | 31 | Modeled | 9.9 |
| 208 | PDV | MO-136 | S-Pad | 240 × 240 | 50.1 | 43.63 | 40.9 | 37.3 | Measured | 9.9 |

## Table 2. SLL Package Thermal-Impedance Data (Continued)

| PIN COUNT | TI PACKAGE | JEDEC SPECIFICATION | PAD SIZE (mils) | CHIP SIZE (mils) | $\theta_{JA}$ (°C/W) AT AIRFLOW (LFM) | | | | MEASURED/ MODELED | $\theta_{JC}$ (°C/W) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0 | 150 | 250 | 500 | | |
| **SOP** | | | | | | | | | | |
| 14 | NS | EIAJ-TYPE-II | 79 × 87 | 55 × 57 | 127.1 | 103.7 | 95.5 | 85.2 | Modeled | 95 |
| 16 | NS | EIAJ-TYPE-II | 87 × 142 | 76 × 86 | 111.3 | 89.3 | 81.4 | 71.5 | Modeled | 95 |
| 20 | NS | EIAJ-TYPE-II | 87 × 118 | 60 × 77 | 100.3 | 82.8 | 76.2 | 68 | Modeled | 90 |
| **TSSOP** | | | | | | | | | | |
| 14 | PW | MO-153 | 71 × 71 | 48 × 53 | 169.8 | 146.7 | 136 | 121.7 | Modeled | 35 |
| 16 | PW | MO-153 | 104 × 104 | 56 × 76 | 148.9 | 127.9 | 117.6 | 103.9 | Modeled | 35 |
| 20 | PW | MO-153 | 102 × 106 | 53 × 69 | 128 | 110.6 | 101.9 | 90.8 | Modeled | 34 |
| 24 | PW | MO-153 | 94 × 140 | 74 × 91 | 119.9 | 98.8 | 90.6 | 80 | Modeled | 33 |
| 48 | DGG | MO-153 | 4.6 × 3.2 mm | 120 × 120 | 89.1 | 78.5 | 75.1 | 69.4 | Measured | 25.2 |
| 56 | DGG | MO-153 | 3.94 × 5.08 mm | 132 × 176 | 81.2 | 72.8 | 65.8 | 57.9 | Modeled | 13 |
| 64 | DGG | MO-153 | 5.7 × 3.6 mm | 120 × 120 | 72.9 | 63.3 | 61.8 | 57.1 | Measured | 21.3 |
| **TVSOP** | | | | | | | | | | |
| 14 | DGV | MO-194 | 75 × 75 | 62 × 62 | 181.5 | 165.8 | 159.5 | 150.4 | Measured | 66.7 |
| 16 | DGV | MO-194 | 75 × 75 | 65 × 65 | 179.6 | 153.2 | 141.7 | 126.3 | Modeled | |
| 20 | DGV | MO-194 | 104 × 104 | 94 × 94 | 146.1 | 122.3 | 111.6 | 97.4 | Modeled | |
| 24 | DGV | MO-194 | 104 × 104 | 94 × 94 | 138.6 | 116.2 | 106.2 | 93.2 | Modeled | |
| 48 | DGV | MO-194 | 100 × 240 | 62 × 186 | 92.9 | 80.9 | 77.1 | 71 | Measured | 27.2 |
| 56 | DGV | MO-194 | 100 × 274 | 90 × 262 | 85.9 | 64.6 | 57.1 | 48.4 | Modeled | |
| 80 | DBB | MO-194 | 100 × 224 | 93 × 203 | 105.6 | 78.4 | 71.8 | 63.7 | Modeled | |
| **PDIP (assumes zero trace length)** | | | | | | | | | | |
| 8 | P | MS-001 | | | 104 | | | | | 41 |
| 14/16 | N | MS-001 | | | 78 | | | | | 32 |
| 20 | N | MS-001 | | | 67 | | | | | 33 |
| 24 | NT | MS-001 | | | 67 | | | | | 25 |
| | | BGA | | | | | | | | |
| 256 | GFN | MO-151 | | | 42 | | | | ANAM data | 6.2 |
| 388 | GFW | MO-151 | | | 18.9 | | | | Model data | |

## Power Calculation

Reduction of power consumption makes a device more robust and reliable. When calculating the total power consumption of a circuit, both the static and the dynamic currents must be taken into account. Both bipolar and BiCMOS devices have varying static-current levels, depending on the state of the output ($I_{CCL}$, $I_{CCH}$, or $I_{CCZ}$), while a CMOS device has a single value for $I_{CC}$. These values can be found in the individual data sheets. TTL-compatible CMOS and BiCMOS inputs, when driven at TTL levels, also consume additional current because they may not be driven all the way to $V_{CC}$ or GND; therefore, the input transistors are not switched completely off. This value, known as $\Delta I_{CC}$, also is provided in the data sheet.

Due to the high operating frequencies, there is a strict limit on power consumption in computer systems. Therefore, allowable power consumption for each device on a board must be minimized. Power calculations are made to determine power-supply sizing, current requirements, cooling/heatsink requirements, and criteria for device selection. Power calculation also can determine the maximum reliable operating frequency.

There are two components that establish the amount of power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

Dynamic power consumption results from charging and discharging external load and internal parasitic capacitances. The parameter for CMOS device parasitic capacitance is $C_{pd}$, which is listed in the data sheet and is obtained using equations 2 and 3:

$$C_{pd} = \frac{I_{CC}}{V_{CC} \times f_i} - C_{L(eff)} \quad (2)$$

$$C_{L(eff)} = C_L \times N_{SW} \times \frac{f_o}{f_i} \quad (3)$$

To explain the $C_{pd}$ and the method of calculating dynamic power, see Table 3, which indicates the $C_{pd}$ test conditions for AHC devices. The symbols used in Table 3 are:

V = $V_{CC}$ (5 V)
G = ground (0 V)
1 = high logic level = $V_{CC}$ (5 V)
0 = low logic level = ground (0 V)
X = don't care: 1 or 0, but not switching
C = 50% duty cycle input pulse (1 MHz) (see Figure 1)
D = 50% duty cycle input (1/2 frequency) out-of-phase input pulse (see Figure 1)
S = standard ac output load (50 pF to GND)

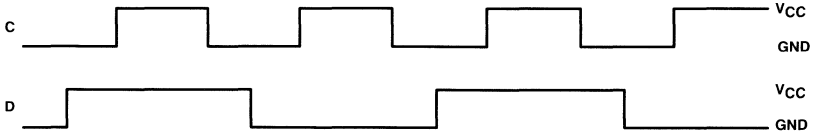



**Figure 1. Input Waveform**

Table 3 shows the switching of each pin for AHC devices. Once the $C_{pd}$ is determined from the table, the $P_D$ is easy to calculate using equations explained in the following sections.

Although a $C_{pd}$ value is not provided for ABT and LVT, the $I_{CC}$ versus frequency curves display essentially the same information (see Figures 2 and 3). The slope of the curve provides a value in the form of mA/(MHz × bit), which when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device without the load current. Equations 4 through 14 can be used to calculate total power for CMOS or BiCMOS devices.

## Table 3. $C_{pd}$ Test Conditions With One- or Multiple-Bit Switching

| TYPE | PIN NO. | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
| AHC00 | C | 1 | S | X | X | S | G | S | X | X | S | X | X | V | | | | | | |
| AHC02 | S | C | 0 | S | X | X | G | X | X | S | X | X | S | V | | | | | | |
| AHC04 | C | S | X | S | X | S | G | S | X | S | X | S | X | V | | | | | | |
| AHC08 | C | 1 | S | X | X | S | G | S | X | X | S | X | X | V | | | | | | |
| AHC10 | C | 1 | X | X | X | S | G | S | X | X | X | S | 1 | V | | | | | | |
| AHC11 | C | 1 | X | X | X | S | G | S | X | X | X | S | 1 | V | | | | | | |
| AHC14 | C | S | X | S | X | S | G | S | X | S | X | S | X | V | | | | | | |
| AHC32 | C | 1 | S | X | X | S | G | S | X | X | S | X | X | V | | | | | | |
| AHC74 | 1 | D | C | 1 | S | S | G | S | S | X | X | X | 1 | V | | | | | | |
| AHC86 | C | 1 | S | X | X | S | G | S | X | X | S | X | X | V | | | | | | |
| AHC138 | C | 0 | 0 | 0 | 0 | 1 | S | G | S | S | S | S | S | S | S | V | | | | |
| AHC139 | 0 | C | 0 | S | S | S | S | G | S | S | S | S | X | X | X | V | | | | |
| AHC240 | 0 | C | S | X | S | X | S | X | S | G | X | S | X | S | X | S | X | S | X | V |
| AHC244 | 0 | C | S | X | S | X | S | X | S | G | X | S | X | S | X | S | X | S | X | V |
| AHC245 | 1 | C | X | X | X | X | X | X | X | G | S | S | S | S | S | S | S | S | 0 | V |
| AHC373† | 0 | S | D | D | S | S | D | D | S | G | C | S | D | D | S | S | D | D | S | V |
| AHC374‡ | 0 | S | D | D | S | S | D | D | S | G | C | S | D | D | S | S | D | D | S | V |
| AHC540 | 0 | C | X | X | X | X | X | X | X | G | S | S | S | S | S | S | S | S | 0 | V |
| AHC541 | 0 | C | X | X | X | X | X | X | X | G | S | S | S | S | S | S | S | S | 0 | V |
| AHC573† | 0 | D | D | D | D | D | D | D | D | G | C | S | S | S | S | S | S | S | S | V |
| AHC574‡ | 0 | D | D | D | D | D | D | D | D | G | C | S | S | S | S | S | S | S | S | V |

† All bits switching, but with no active clock signal
‡ All bits switching

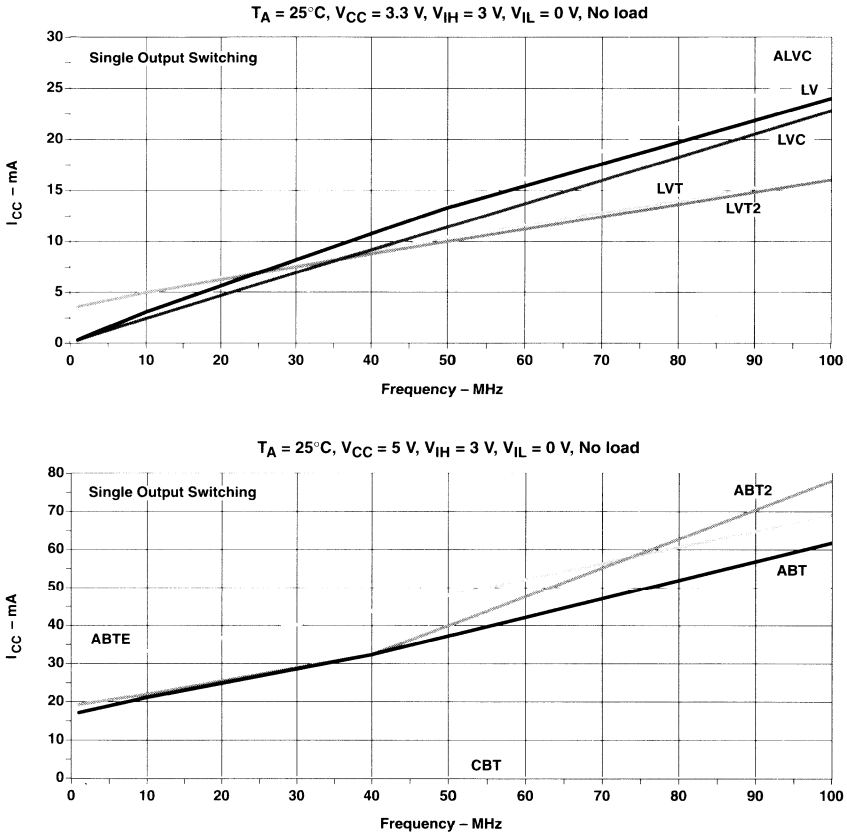



**Figure 2. Power Consumption With a Single Output Switching**

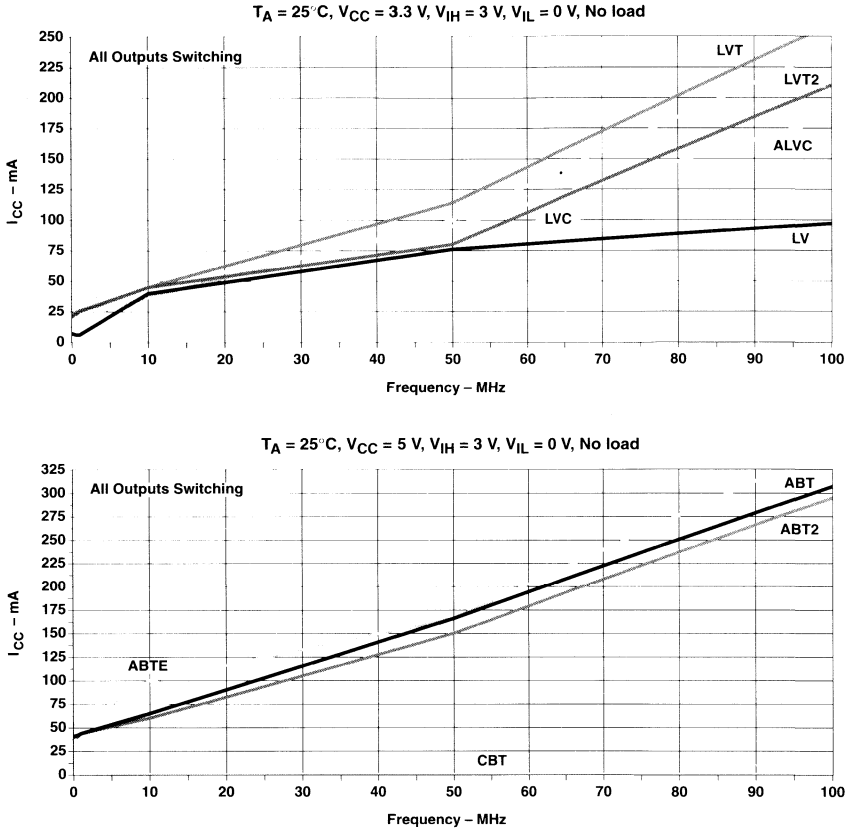



**Figure 3. Power Consumption With All Outputs Switching**

## CMOS

### *CMOS-Level Inputs*

Static power consumption can be calculated using equation 4.

$$P_S = V_{CC} \times I_{CC} \tag{4}$$

The dynamic power consumption of a CMOS device is calculated by adding the transient power consumption and capacitive-load power consumption.

### *Transient Power Consumption*

The transient power is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This power is a result of the current required to charge the internal nodes (*switching current*) plus the current that flows from $V_{CC}$ to GND when the p-channel and n-channel transistors turn on briefly at the same time during the logic transition (*through current*). The frequency at which the device is switching, plus the rise and fall time of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible in comparison with the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the device and the charge and discharge current of the load capacitance.The transient power consumption can be calculated using equation 5.

$$P_T = C_{pd} \times V_{CC}{}^2 \times f_I \times N_{SW} \quad (5)$$

In case of single-bit switching, $N_{SW}$ in equation 5 becomes 1.

### *Capacitive-Load Power Consumption*

Additional power is consumed in charging of external load capacitance and is dependent on switching frequency. Equation 6 can be used to calculate this power while all outputs have the same load and are switching at the same output frequency.

$$P_L = C_L \times V_{CC}{}^2 \times f_O \times N_{SW} \text{ ($C_L$ is the load per output)} \quad (6)$$

In case of different loads and different output frequencies at all outputs, equation 7 is used to calculate capacitive-load power consumption.

$$P_L = \Sigma(C_{Ln} \times f_{On}) \times V_{CC}{}^2 \quad (7)$$

Therefore, dynamic power consumption ($P_D$) is the sum of these two power consumptions, and is expressed in equation 8 (single-bit-switching case) and 9 (multiple-bit switching with variable load and variable output frequencies):

$$P_D = (C_{pd} \times f_I \times V_{CC}{}^2) + (C_L \times f_O \times V_{CC}{}^2) \quad (8)$$

$$P_D = [(C_{pd} \times f_I \times N_{SW}) + \Sigma(C_{Ln} \times f_{On})]V_{CC}{}^2 \quad (9)$$

Total power consumption with a CMOS-level input is the sum of static and dynamic power consumption.

### *TTL-Level Inputs*

Similarly, with TTL-level inputs, both static and dynamic power consumption can be calculated using equations 10, 11, and 12.

$$P_S = V_{CC}[I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)] \quad (10)$$

$$P_D = (C_{pd} \times f_I \times V_{CC}{}^2) + (C_L \times f_O \times V_{CC}{}^2) \text{ (single-bit switching)} \quad (11)$$

$$P_D = [(C_{pd} \times f_I \times N_{SW}) + \Sigma(C_{Ln} \times f_{On})]V_{CC}{}^2 \quad (12)$$

(multiple-bit switching with variable load and frequency)

## BiCMOS

### *Static Power*

$$P_S = V_{CC}\left\{DC_{en}\left[\left(N_H \times \frac{I_{CCH}}{N_T}\right) + \left(N_L \times \frac{I_{CCL}}{N_T}\right)\right] + (1 - DC_{en})I_{CCZ} + (N_{TTL} \times \Delta I_{CC} \times DC_d)\right\} \quad (13)$$

Where:

$\Delta I_{CC} = 0$ for bipolar devices

**NOTE:**
For a continuous waveform at 50% duty cycle, $DC_{en} = 1$.

Equation 13 becomes:

$$P_S = V_{CC}\left[\left(N_H \times \frac{I_{CCH}}{N_T}\right) + \left(N_L \times \frac{I_{CCL}}{N_T}\right)\right] \quad (14)$$

**NOTE:**

If half of the time the waveform is high and half of the time the waveform is low and the waveform is switching continuously, $\Rightarrow (N_H = N_L = 1/2\ N_T)$, $P_S$ becomes:

$$P_S = \left(\frac{V_{CC}}{2}\right)(I_{CCH} + I_{CCL}) \quad (15)$$

### *Dynamic Power*

$$P_D = (DC_{en} \times N_{SW} \times V_{CC} \times f \times I_{CCD}) \text{ Condition is } 50 \text{ pF} \parallel 500\ \Omega \quad (16)$$

$I_{CCD}$ is calculated with 50 pF ‖ 500 Ω, and given number of outputs switching.

**NOTE:**

For a continuous waveform at 50% duty cycle, $DC_{en} = 1$.

Dynamic power with external capacitance:

$$P_D = DC_{en} \times N_{SW} \times V_{CC} \times f \times (V_{OH} - V_{OL}) \times (C_L - 50 \text{ pF}) + DC_{en} \times N_{SW} \times V_{CC} \times f \times I_{CCD} \quad (17)$$

$I_{CCD}$ is calculated with 50 pF ‖ 500 Ω, and given number of output switching.

Power is also consumed by the upper output driver due to the output resistor (500 Ω in most load circuits for outputs in the data sheet). This power is very small but must be included in the dynamic power consumption calculation. Equation 18 is used to calculate this power consumption.

$$P_{Res} = (V_{CC} - V_{OH}) \times \frac{V_{OH}}{R} \quad (18)$$

**NOTE:**

Assume that the output waveform is always at logic high and is not frequency dependent.

Therefore, total dynamic power consumption is:

$$P_{D\ TOT} = P_D + P_{Res} \quad (19)$$

Finally, total power consumption can be calculated as:

$$P_{Total} = P_{D\ TOT} + P_S \quad (20)$$

Where:

$V_{CC}$ = supply voltage (V)
$I_{CC}$ = power-supply current (A) (from the data sheet)
$I_{CCL}$ = power-supply current when outputs are in low state (A) (from the data sheet)
$I_{CCH}$ = power-supply current when outputs are in high state (A) (from the data sheet)
$I_{CCZ}$ = power-supply current when outputs are in high-impedance state (A) (from the data sheet)
$\Delta I_{CC}$ = power-supply current when one input is at a TTL level (A) (from the data sheet)
$DC_{en}$ = % duty cycle enabled (50% = 0.5)

$DC_d$ = % duty cycle of the data (50% = 0.5)
$N_H$ = number of outputs in high state
$N_L$ = number of outputs in low state
$N_{sw}$ = total number of outputs switching
$N_T$ = total number of outputs

$N_{TTL}$ = number of inputs driven at TTL levels

$f_I$ = input frequency (Hz)
$f_O$ = output frequency (Hz)
$f$ = operating frequency (Hz)
$V_{OH}$ = output voltage in high state (V)
$V_{OL}$ = output voltage in low state (V)
$C_L$ = external-load capacitance (F)
$I_{CCD}$ = slope of the $I_{CC}$ versus frequency curve (A/Hz × bit)

$C_{L(eff)}$ = effective-load capacitance (F)
$f_O/f_I$ = ratio of output and input frequency (Hz)
$P_T$ = transient power consumption
$P_D$ = dynamic power consumption
$P_S$ = static power consumption
$P_{\_Res}$ = power consumption due to output resistance
$P_{D\_TOT}$ = total dynamic power consumption
$P_{\_Total}$ = total power consumption

$C_{PD}$ = dynamic power dissipation capacitance (F)
$P_L$ = capacitive-load power consumption
$\Sigma$ = sum of n different frequencies and loads at n different outputs
$f_{On}$ = all different output frequencies at each output numbered 1 through n (Hz)
$C_{Ln}$ = all different load capacitances at each output numbered 1 through n

For GTL and BTL/FB devices, the power consumption/calculation is similar to a BiCMOS device with the addition of the output power consumption through the pullup resistor, since GTL is open drain and BTL/FB is open collector.

The total power calculated using these equations should be less than the package power dissipation mentioned in the data sheets. Otherwise, the device might not function properly.

## Benefits of Minimizing Power Consumption

Power consumption can be minimized in a number of ways. DC power consumption can be reduced to leakage by using only CMOS logic, as opposed to bipolar and BiCMOS logic. The leakage, in turn, is proportional to the area of diffusion, so the use of minimum-size devices is an advantage. Dynamic power consumption can be limited by reducing supply voltage, switched capacitance, and the frequency at which the logic is clocked. Supply voltage tends to be a system design consideration, and low-power systems use 1.5-V to 3.3-V supplies.

Power consumption is a function of the load capacitance, the frequency of operation, and the supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several other benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heatsinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower-temperature stress gradients on the device, and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.

## Reliability Implications

The integrated-circuit component power dissipation during operation elevates the device junction temperature. The thermal impedance ($\theta_{JA}$ or k-factor) of a device package is defined as the increase in the junction temperature, above ambient temperature, due to the device power dissipation. Thermal impedance is measured in degrees Celsius per watt. Thermal characteristics of a device package are commonly described using two indices, $Q_{JA}$ (junction to ambient) and $Q_{JC}$ (junction to case). Controlling the junction temperature within a desired range is critical for proper device functionality and long-term reliability.

Table 4, based on long-term sustained temperatures, shows the relationship between junction temperature and predicted failure rate.

**Table 4. Junction Temperature Versus 100,000-Hour Predicted Failure Rate**

| JUNCTION TEMPERATURE (°C) | FAILURE RATE (%) |
|---|---|
| 100 | 0.02 |
| 110 | 1 |
| 120 | 11 |
| 130 | 46 |
| 140 | 80 |
| 150 | 96 |

Higher component temperatures increase the possibility of component wearout due to such failure mechanisms as electromigration and ball-bond intermetallic failures.

### Thermal Definitions

*Heat* — A form of energy associated with the motion of atoms or molecules in solids, and capable of being transmitted through solid and fluid media by conduction, through fluid media by convection, and through empty space by radiation

*Conduction Heating* — The most commonly recognized form of heat transfer. Metal materials are good conductors of heat and can be quantified by a proportionality constant (k), also known as thermal conductivity. The higher the thermal-conductivity number, the more quickly heat transfer, by means of conduction, occurs. Leadframes are the primary media for conduction heating in plastic-encapsulated devices; however, mold compound materials play a major role in this type of heat transference.

*Convection Heating* — The heat transfer by fluid motion between regions of unequal density that result from nonuniform heating. This type of heat transfer is most commonly seen when air is forced across a heated surface, resulting in the cooling of the heat source. Heat is transferred to the air by means of convection heating. The rate of heat transfer depends on the surface area of the heat source and the velocity and physical properties of the airflow. When a device package is generating heat through normal operation, the device can be cooled by applying a constant airflow across the surface of the package.

*Radiation* — Radiant heat transfer occurs between two objects separated within a vacuum.

*Ambient Temperature* — The temperature of the surrounding air, usually used as a reference point to calculate the junction or case temperature. This temperature is measured at some specific distance from the device.

*Case Temperature* — The temperature on the package surface measured at the center of the top of the package

*Junction Temperature* — The temperature of the die inside the device package

## Acknowledgment

The authors of this report are David Holmgreen, Doug Romm, Abul Sarwar, and Ron Eller. The thermal-model program, ThermCAL, was developed by Darvin Edwards.

## References

1 Electronic Industries Association, EIA/JEDEC Std JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, August 1996.

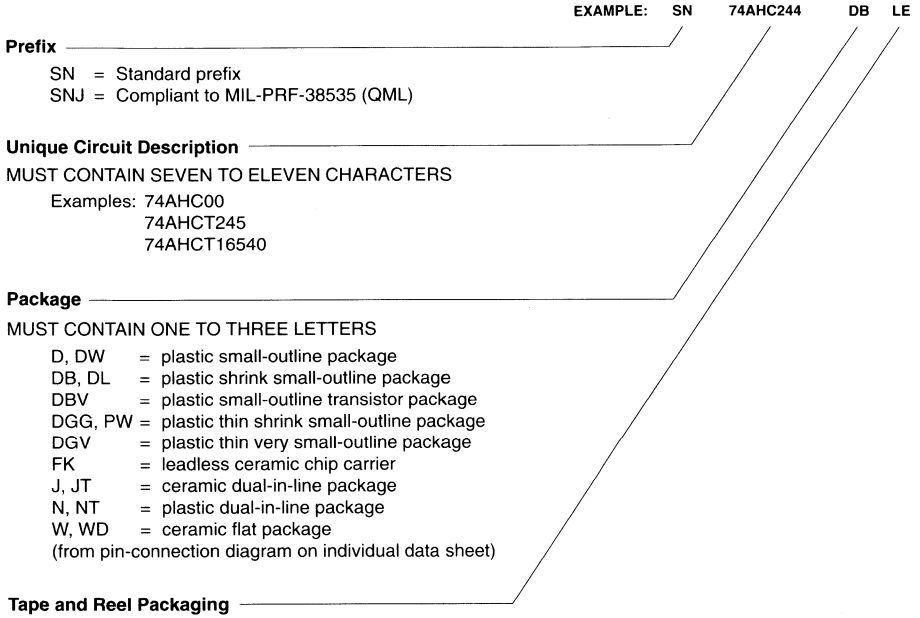
2 Darvin Edwards, "Thermal Analysis Using FEA (v1.1)," November 1991.

3 Darvin Edwards, "Development of JEDEC Standard Thermal Measurement Test Boards."

## Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as explained in the following example.




Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE OR TWO LETTERS

LE = Left embossed tape and reel (required for DB and PW packages)
R = Standard tape and reel (required for DGG and DGV; optional for D, DL, and DW packages)

The purpose of tape-and-reel packing is to position components so they can be placed automatically. Components such as, but not limited to, diodes, capacitors, resistors, transistors, inductors, and integrated circuits can be packed in this manner.

The packing materials include a carrier tape, cover tape, and a reel. The normal dimensions for these items are listed in Table 1.

**Table 1. Normal Dimensions of Packing Materials**

| CARRIER-TAPE WIDTH (mm) | COVER-TAPE WIDTH (mm) | REEL WIDTH (mm) | REEL DIAMETER (mm) |
|---|---|---|---|
| 12 | 9.2 | 12.4 | 330 |
| 16 | 13.3 | 16.4 | 330 |
| 24 | 21.0 | 24.4 | 330 |
| 32 | 25.5 | 32.4 | 330 |
| 44 | 37.5 | 44.4 | 330 |
| 56 | 49.5 | 56.4 | 330 |

All material meets or exceeds industry guidelines for ESD protection.

Dimensions are selected based on package size and design configurations. All dimensions are established to be within the recommendations of the Electronics Industry Association Standard EIA-481-1,2,3.

Common dimensions of particular interest to the end user are carrier-tape width, pocket pitch, and quantity per reel (see Figure 1 and Table 2).

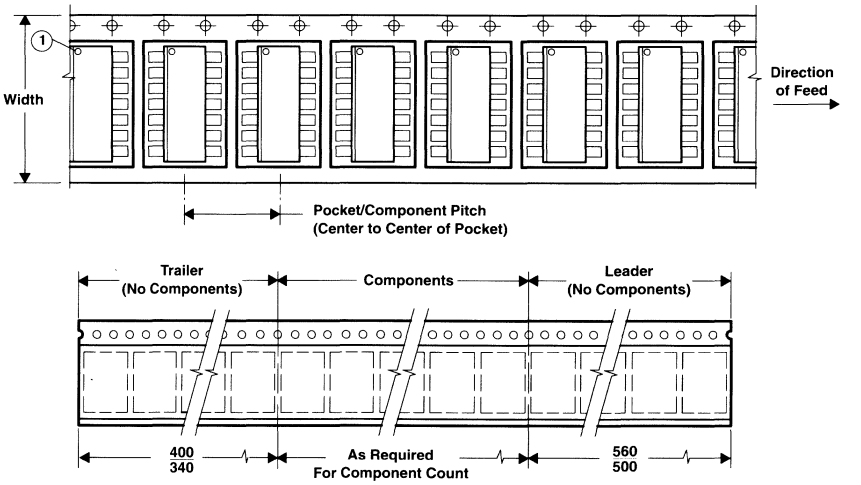



**Figure 1. Typical Carrier-Tape Design**



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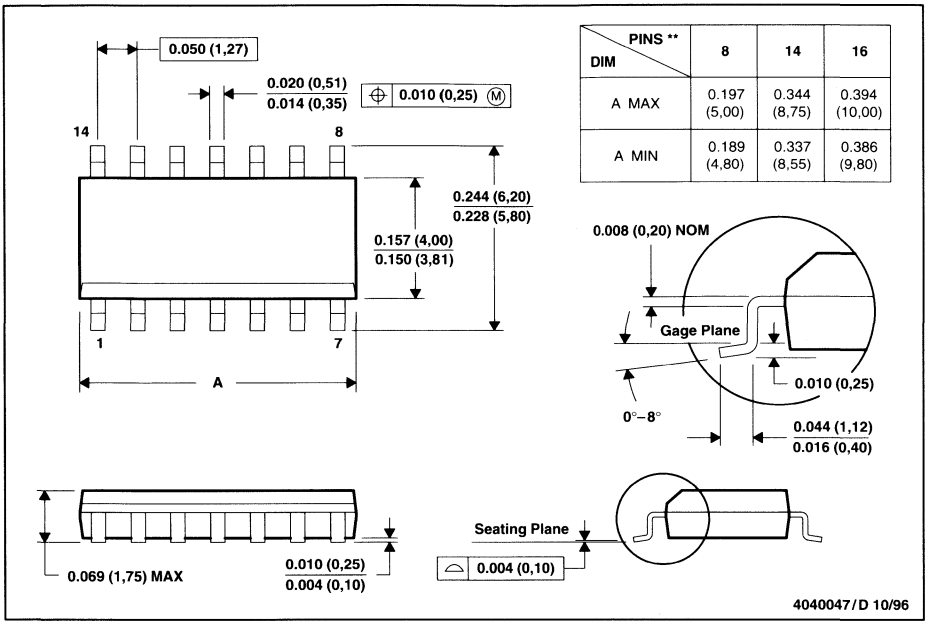
**Table 2. Selected Tape and Reel Specifications**

| PACKAGE | | NO. OF PINS | CARRIER-TAPE WIDTH (mm) | POCKET PITCH (mm) | QTY/REEL |
|---|---|---|---|---|---|
| SOIC | D | 14 | 16.00 | 8.00 | 2500 |
| | | 16 | 16.00 | 8.00 | 2500 |
| | DW | 16 | 16.00 | 8.00/12.00 | 1000 |
| | | 20 | 24.00 | 12.00 | 1000 |
| SSOP | DB | 14/16 | 16.00 | 12.00 | 2000 |
| | | 20 | 16.00 | 12.00 | 2000 |
| | DL | 48 | 32.00 | 16.00 | 1000 |
| TSSOP | DGG | 48 | 24.00 | 12.00 | 2000 |
| | PW | 8 | 16.00 | 8.00 | 2000 |
| | | 14/16 | 16.00 | 8.00 | 2000 |
| | | 20 | 16.00 | 8.00 | 2000 |
| TVSOP | DGV | 14 | 16.00 | 8.00 | 2000 |
| | | 16 | 16.00 | 8.00 | 2000 |
| | | 20 | 16.00 | 8.00 | 2000 |
| | | 48 | 16.00 | 8.00 | 2000 |

## D (R-PDSO-G**)

## PLASTIC SMALL-OUTLINE PACKAGE

**14 PIN SHOWN**

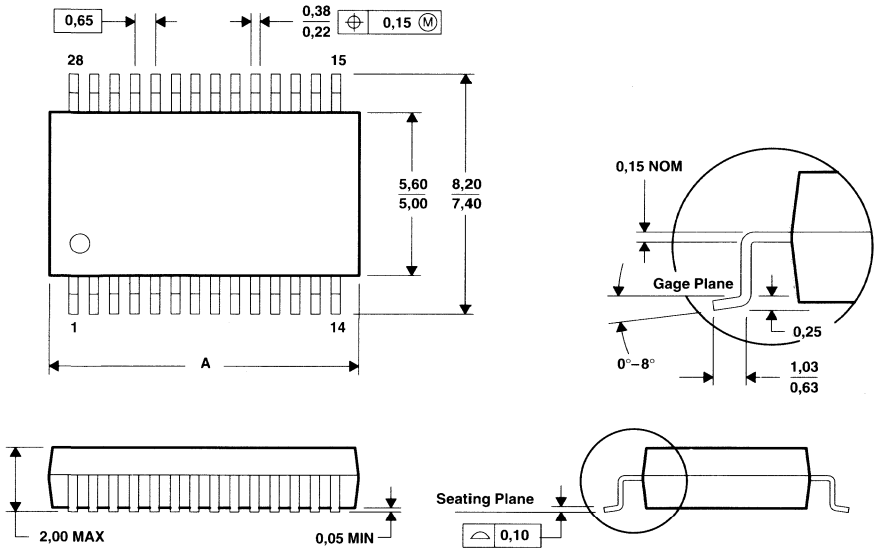



| DIM \ PINS ** | 8 | 14 | 16 |
|---|---|---|---|
| A MAX | 0.197 (5,00) | 0.344 (8,75) | 0.394 (10,00) |
| A MIN | 0.189 (4,80) | 0.337 (8,55) | 0.386 (9,80) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**28 PIN SHOWN**

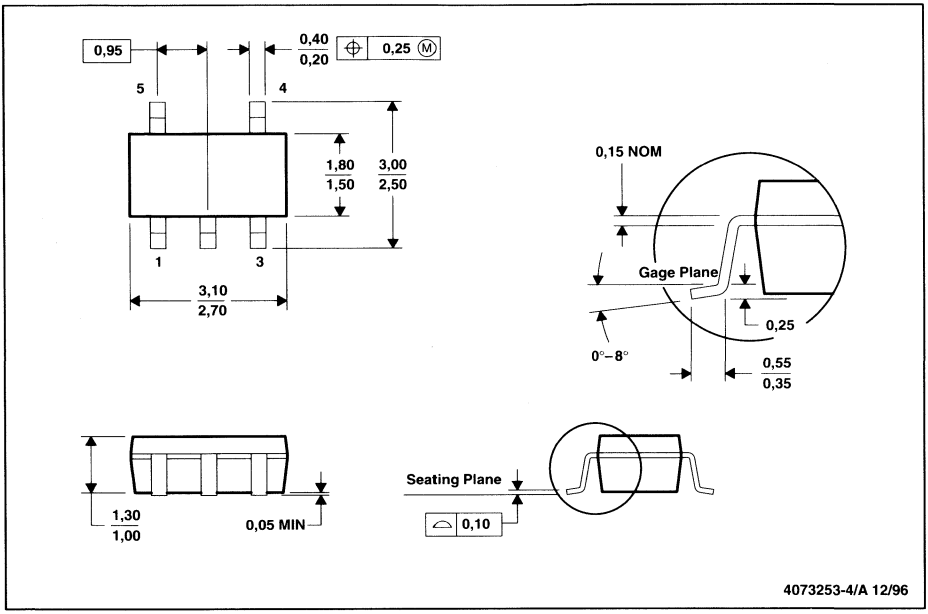



| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|---|
| A MAX | 3,30 | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 2,70 | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 / C 10/95**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

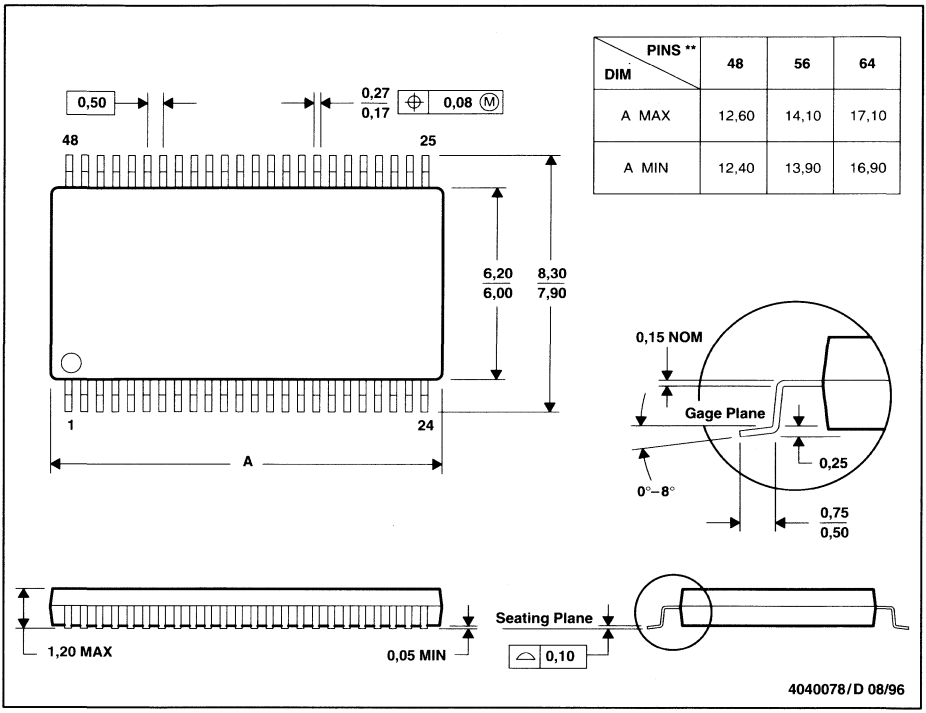
**DBV (R-PDSO-G5)** **PLASTIC SMALL-OUTLINE PACKAGE**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PIN SHOWN**

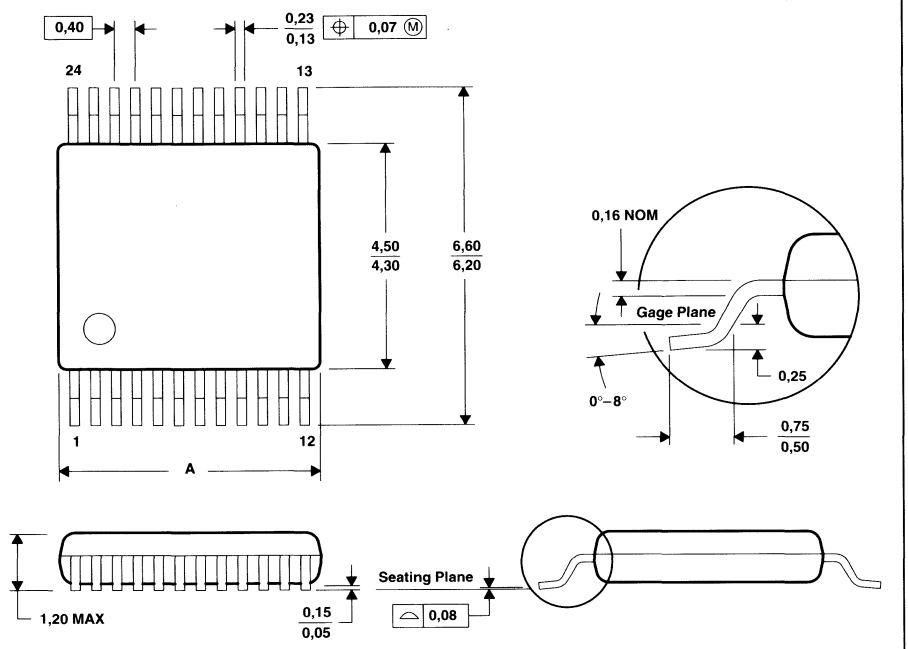



| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-153

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**24 PIN SHOWN**



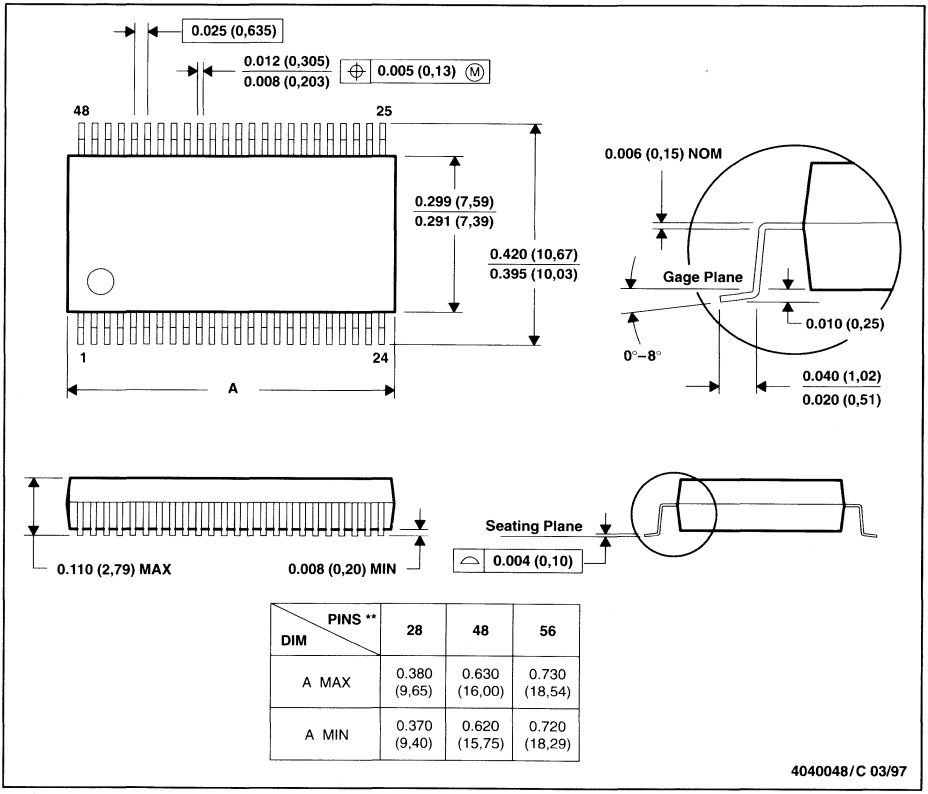

| DIM \ PINS ** | 14 | 16 | 20 | 24 | 48 | 56 |
|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 9,60 | 11,20 |

**4073251/b 03/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. The 24 and 48 pins falls within JEDEC MO-153 and the 14, 16, 20, and 56 pins falls within JEDEC MO-194.

**DL (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PIN SHOWN**




| DIM \ PINS ** | 28 | 48 | 56 |
|---|---|---|---|
| A MAX | 0.380 (9,65) | 0.630 (16,00) | 0.730 (18,54) |
| A MIN | 0.370 (9,40) | 0.620 (15,75) | 0.720 (18,29) |

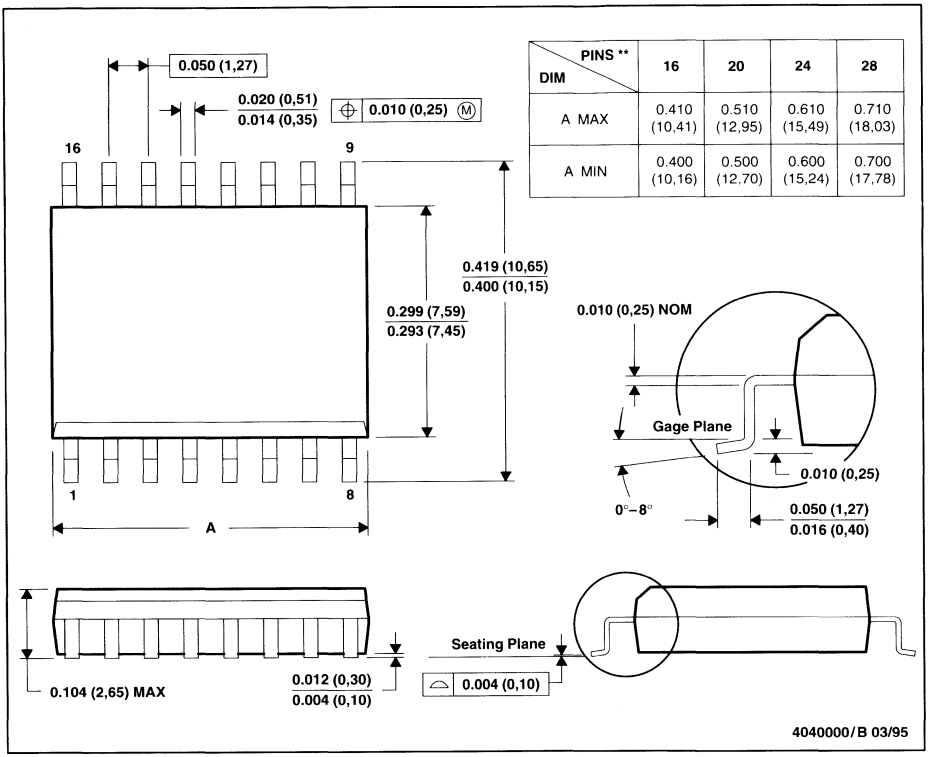
4040048/C 03/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

## DW (R-PDSO-G**)

## PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN

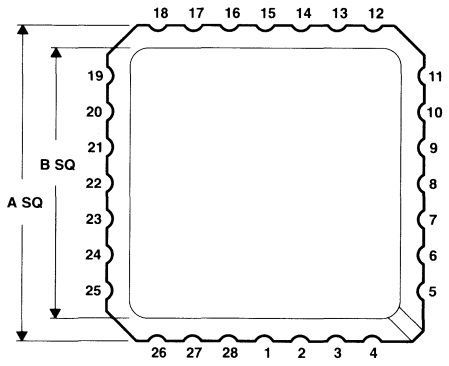



| DIM \ PINS ** | 16 | 20 | 24 | 28 |
|---|---|---|---|---|
| A MAX | 0.410 (10,41) | 0.510 (12,95) | 0.610 (15,49) | 0.710 (18,03) |
| A MIN | 0.400 (10,16) | 0.500 (12,70) | 0.600 (15,24) | 0.700 (17,78) |

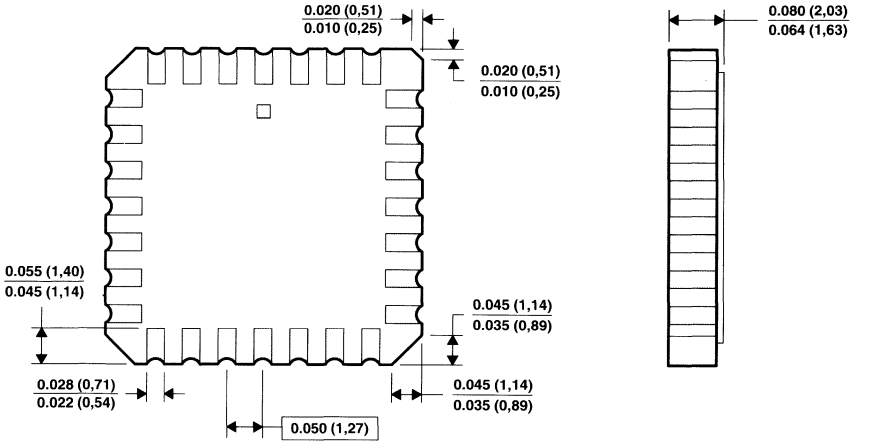
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

**FK (S-CQCC-N**)** **LEADLESS CERAMIC CHIP CARRIER**

**28 TERMINAL SHOWN**




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.739 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |

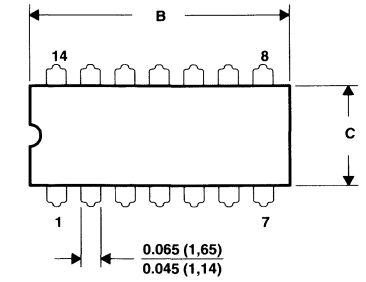



4040140/D 10/96

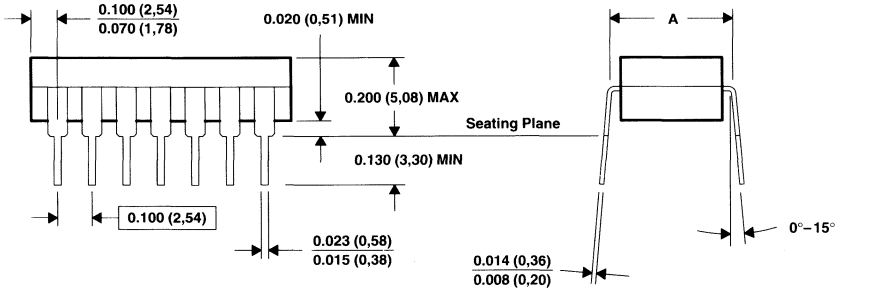
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

**J (R-GDIP-T**)** **CERAMIC DUAL-IN-LINE PACKAGE**

**14 PIN SHOWN**




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.310 (7,87) | 0.310 (7,87) | 0.310 (7,87) | 0.310 (7,87) |
| A MIN | 0.290 (7,37) | 0.290 (7,37) | 0.290 (7,37) | 0.290 (7,37) |
| B MAX | 0.785 (19,94) | 0.785 (19,94) | 0.910 (23,10) | 0.975 (24,77) |
| B MIN | 0.755 (19,18) | 0.755 (19,18) | — | 0.930 (23,62) |
| C MAX | 0.280 (7,11) | 0.300 (7,62) | 0.300 (7,62) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.245 (6,22) | 0.245 (6,22) |

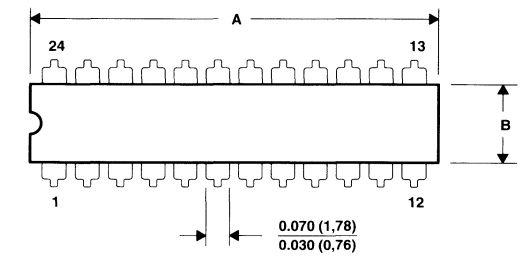



4040083/C 08/96

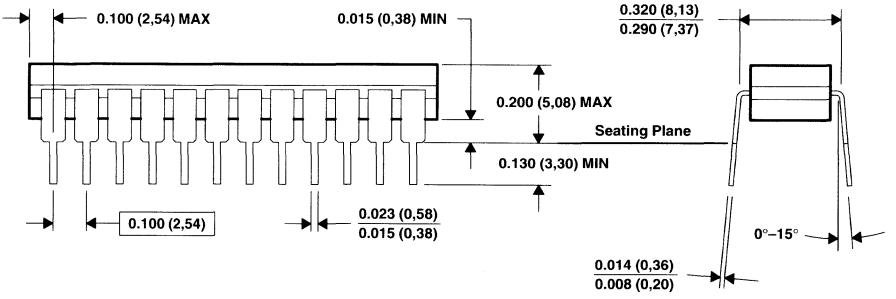
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, and GDIP1-T20

**JT (R-GDIP-T**)** **CERAMIC DUAL-IN-LINE PACKAGE**

**24 PIN SHOWN**




| DIM \ PINS** | 24 | 28 |
|---|---|---|
| A MAX | 1.280 (32,51) | 1.460 (37,08) |
| A MIN | 1.240 (31,50) | 1.440 (36,58) |
| B MAX | 0.300 (7,62) | 0.291 (7,39) |
| B MIN | 0.245 (6,22) | 0.285 (7,24) |



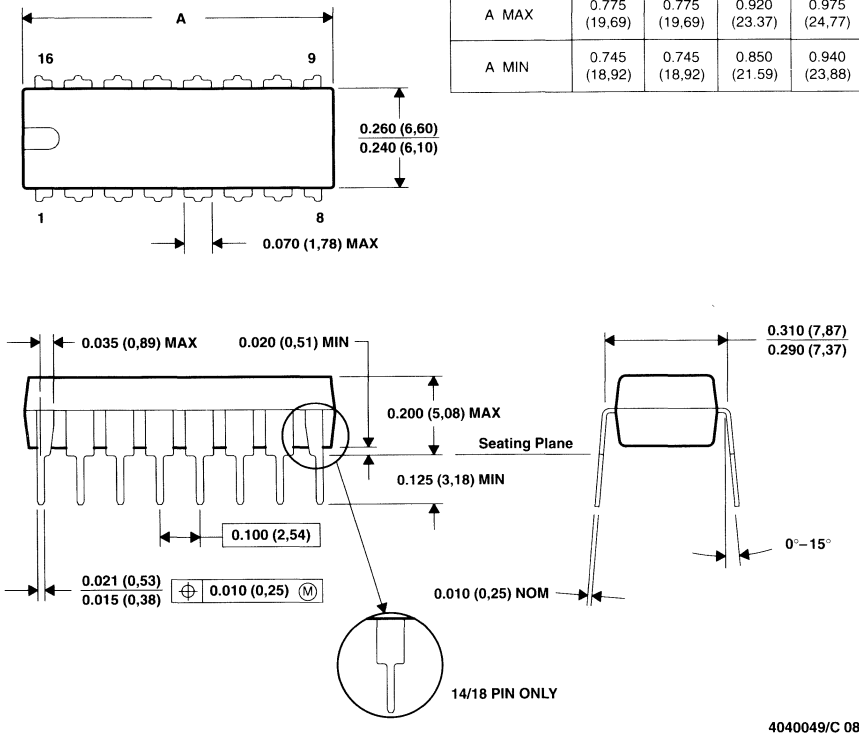

4040110/C 08/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP-T24, GDIP-T28 and JEDEC MO-058 AA, MO-058 AB.

**N (R-PDIP-T**)** **PLASTIC DUAL-IN-LINE PACKAGE**

**16 PIN SHOWN**

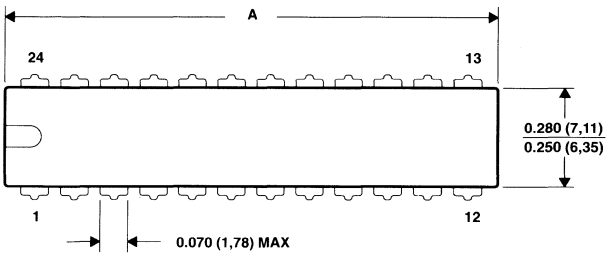
| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23.37) | 0.975 (24,77) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21.59) | 0.940 (23,88) |



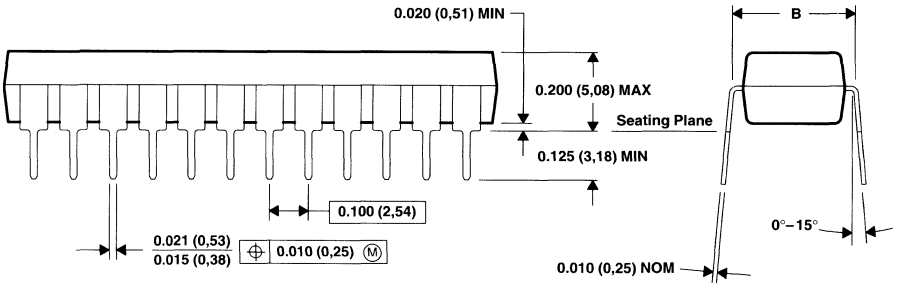

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

**NT (R-PDIP-T**)** **PLASTIC DUAL-IN-LINE PACKAGE**

**24 PIN SHOWN**




| DIM \ PINS ** | 24 | 28 |
|---|---|---|
| A MAX | 1.260 (32,04) | 1.425 (36,20) |
| A MIN | 1.230 (31,24) | 1.385 (35,18) |
| B MAX | 0.310 (7,87) | 0.315 (8,00) |
| B MIN | 0.290 (7,37) | 0.295 (7,49) |

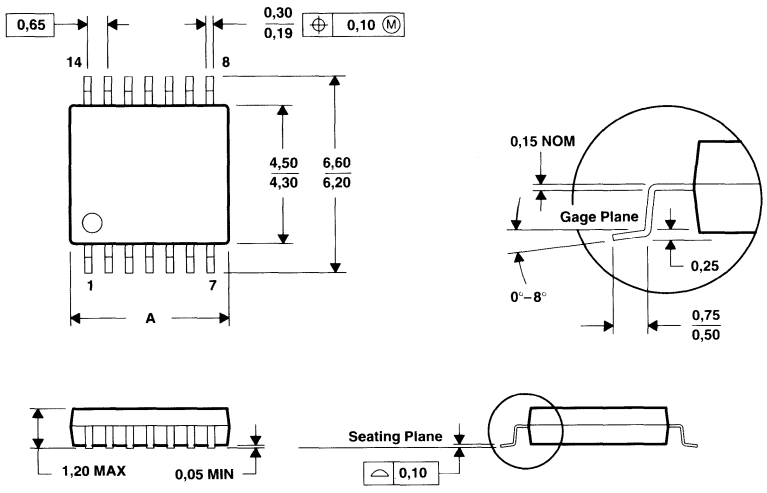



4040050/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PIN SHOWN**

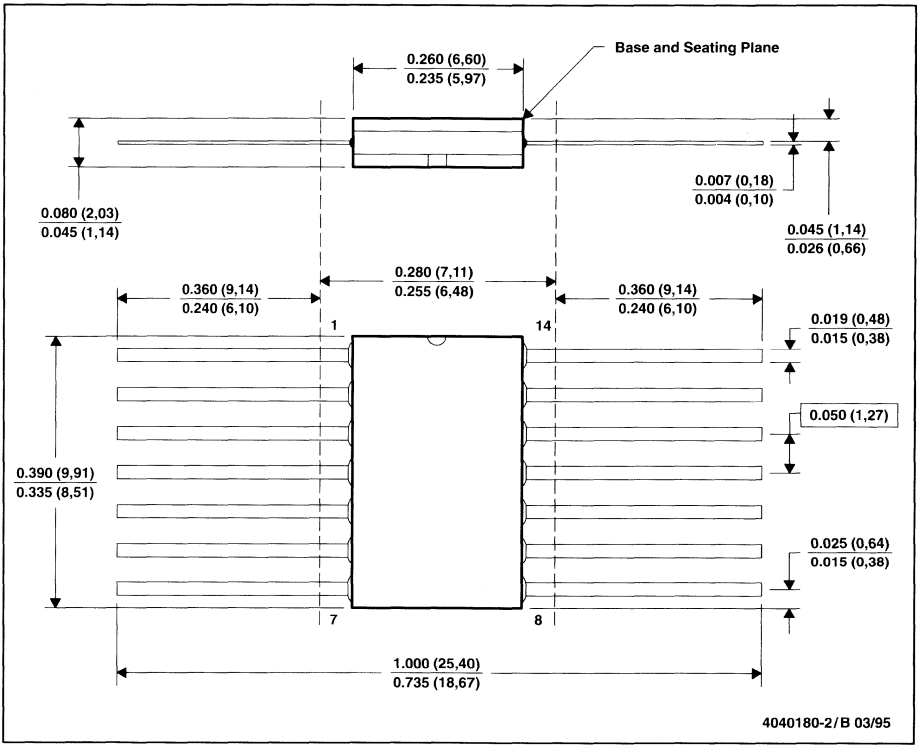



| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/E 08/96**

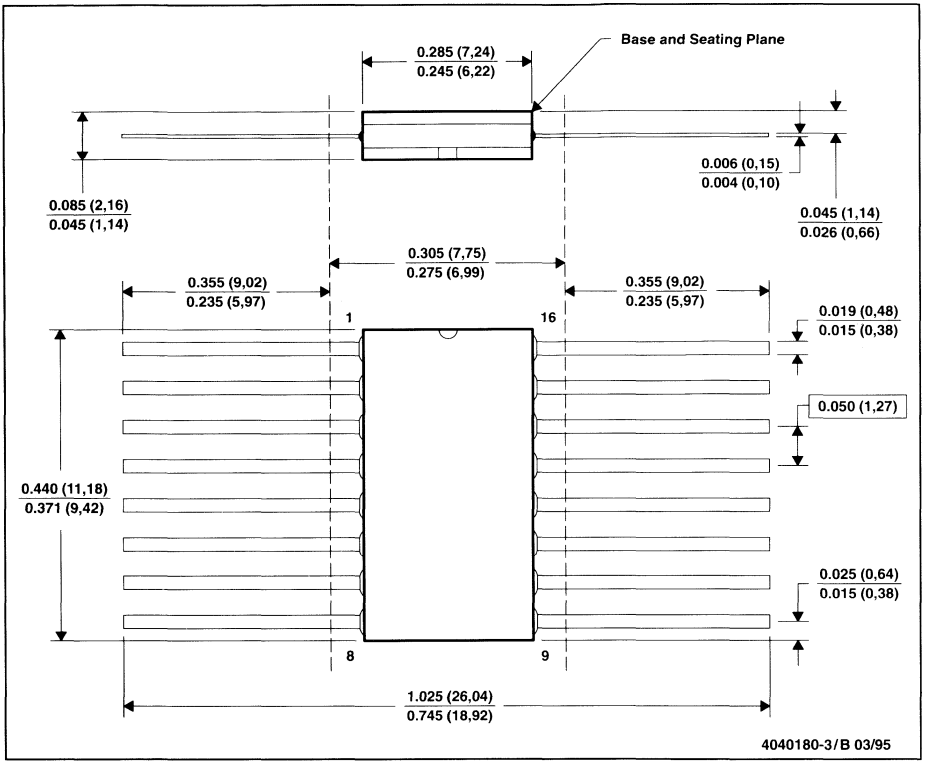
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

**W (R-GDFP-F14)** **CERAMIC DUAL FLATPACK**



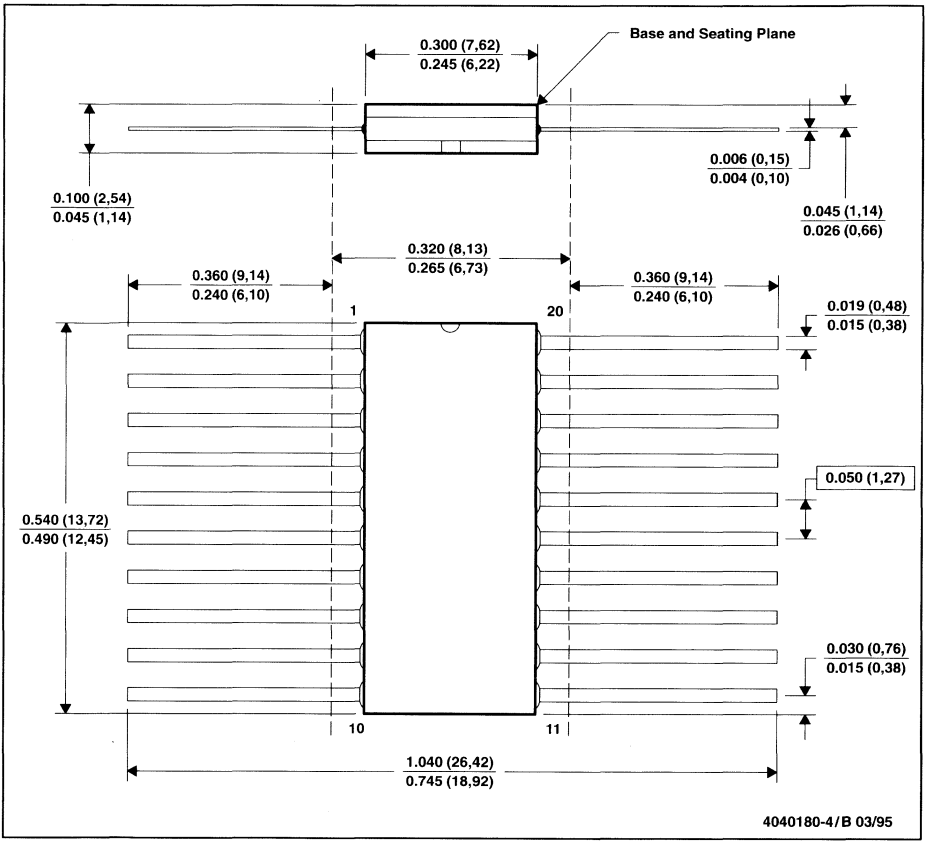

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

**W (R-GDFP-F16)** **CERAMIC DUAL FLATPACK**



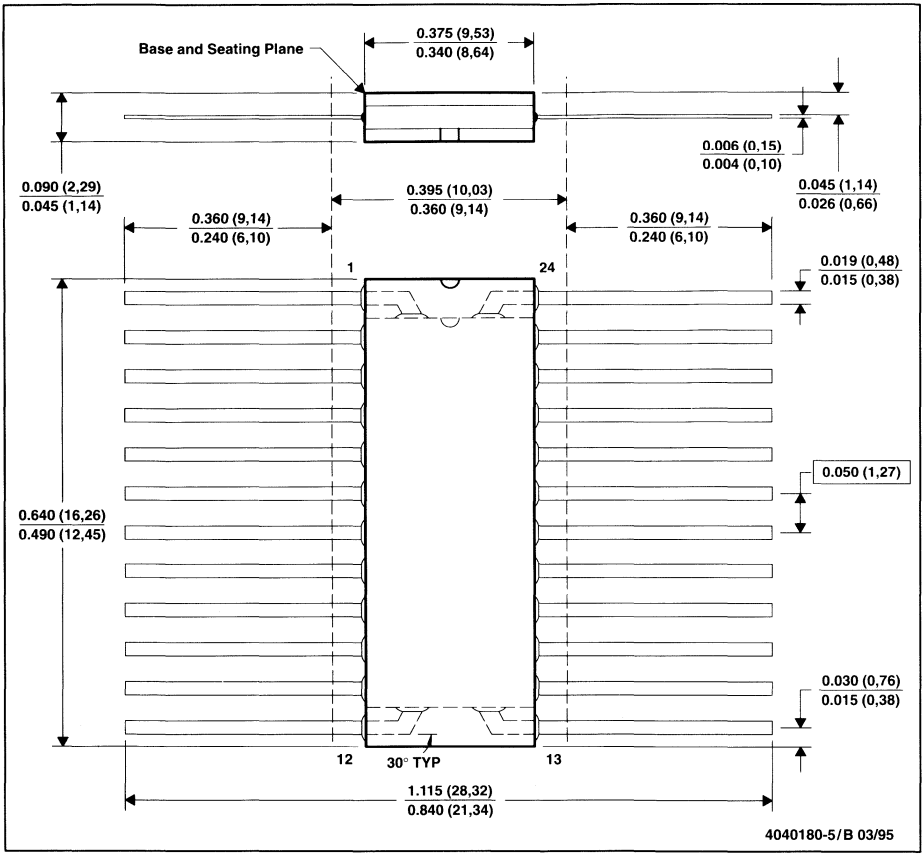

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL-STD-1835 GDFP1-F16 and JEDEC MO-092AC

**W (R-GDFP-F20)** **CERAMIC DUAL FLATPACK**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL-STD-1835 GDFP2-F20

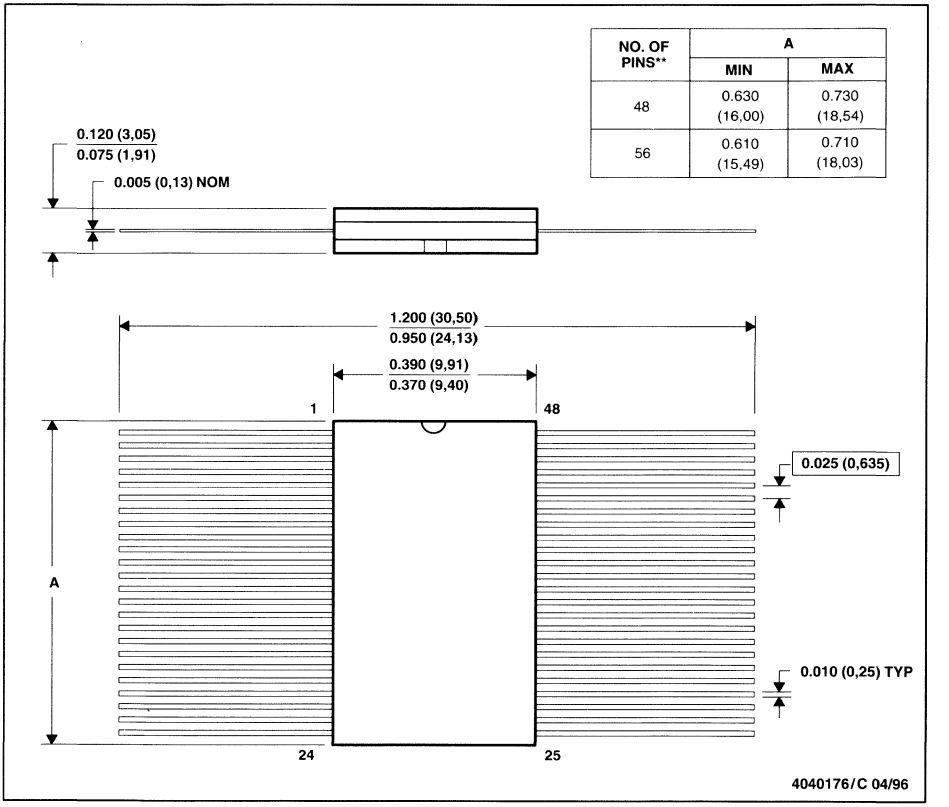
**W (R-GDFP-F24)** **CERAMIC DUAL FLATPACK**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
E. Index point is provided on cap for terminal identification only.

**WD (R-GDFP-F**)** **CERAMIC DUAL FLATPACK**

**48 PIN SHOWN**




| NO. OF PINS** | A | |
|---|---|---|
| | MIN | MAX |
| 48 | 0.630 (16,00) | 0.730 (18,54) |
| 56 | 0.610 (15,49) | 0.710 (18,03) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for pin identification only
E. Falls within MIL-STD-1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

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